WANG

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CUSTOMER ENGINEERING

PRODUCT MAINTENANCE MANUAL

WANG WRITER
MODEL 5503

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CHAPTER 1
INTRODUCTION

This service manual for the Wangwriter, Model 5503, contains information pertaining to the servicing of the Wangwriter at a field level of maintenance. In some instances, where noted, the information may pertain to maintenance at a higher level.

1.1 SYSTEM OVERVIEW

The Wangwriter is a "standalone" system for word processing; the system is self contained in that it comprises all the components necessary for both the visual text processing and the printing of a document. Three principal units compose the system: a display terminal, a moveable keyboard, and a printer console containing a single minidiskette drive.

The display terminal consists of a CRT (12-inch diagonal) capable of displaying 80 characters by 24 lines of text. Horizontal scrolling provides a 158-character maximum scrolling capability.

The keyboard consists of a standard typewriter keyboard, with the addition of separate operational keys and a cursor movement key pad.

The printer console contains the printer assembly, the minidiskette drive, and the major portion of the system electronics. The printer uses standard daisy printer wheels, and can offer a choice of typing pitches of 10, 12, and 15 characters per inch, in a variety of print styles. Further, the printer can accomodate a choice of either six or eight lines thus providing the correct vertical proportion for the desired horizontal pitch.

The Wangwriter is a document-oriented system with single-page access; the software allows random access to any given page within a specified document. Each archival minidiskette can contain 330,000 characters, or approximately 130 pages of information.

1.2 SPECIFICATIONS

The following table provides a summary of system capabilities and operational characteristics.

WORKSTATION/KEYBOARD

Physical Dimensions

Height .....15.0 in (38.1 cm)
Depth .....12.8 in (32.5 cm)
Width .....13.5 in (34.3 cm)

Approximate Net Weight
28 lb (12.72 kg)

Display Size
12 in. diagnonal (30.4 cm)

Character Size
Height .....0.16 in (0.41 cm)
Width .....0.09 in (0.23 cm)

Capacity
24 lines, 80 characters/line

Controls
Contrast
Brightness

Cabling
10 ft (3.0 m) - workstation to printer

Keyboard
Standard Typewriter Keys
4 Cursor Control Keys
22 Special Operational Keys
Repeat Keys: cursor keys, space bar, backspace, attribute keys

Cabling
10 ft. (3.0 m) keyboard to printer

PRINTER

Physical Dimensions

Height .....26.8 in (68.1 cm)
Depth .....12.0 in (30.5 cm)
Width .....22.0 in (55.9 cm)

Approximate Net Weight
73 lb (33.18 kg)

Speed
20 characters per second average, bidirectional

Pitch/Line Length (11")

10 pitch -- 110 characters
12 pitch -- 132 characters
15 pitch -- 165 characters

Paper Specifictions

Minimum Width .....3.5 in (8.9 cm)
Maximum Width .....11.69 in (29.7 cm)

Paper Thickness

0.027 in. (0.069 cm) (5 copies, plus original)

Character Set

Standard characters
Special characters plus additional characters created by overstriking

Control Panel

Indicator: Power, Change Daisy Change Ribbon, Change Paper, Indicators
Switches: Line Feed Up, Line Feed Down, Roll Up, Roll Down, Select, Top of Page.

Lamps

MALFUNCTION

Ribbon Cartridges

Carbon multistrike
Carbon singlestrike

Print Wheels

10-Pitch	12-Pitch	15-Pitch
Courier	Courier	Cubic
Delegate	Elite	Letter Gothic
Narrator	Letter Gothic	
OCR A	Prestige Elite	
OCR B	Scientific Gothic	
Prestige Pica		
Symbol		

Cabling

8 to 6 ft (3.0 m) printer to power source

Power Requirements

115 or 230 VAC + 10% - 15%
50 or 60 Hz $\pm$ 1 Hz
-300 watts

Fuses

3A S.B. @ 115 VAC
1.5A S.B. @ 230 VAC

Operating Environment

50 F to 90 F (10 C to 32 C)
20% to 80% relative humidity, noncondensing
(recommended 35% to 65%)

Mini-Floppy Disk Drive

Media	5 1/4 inch floppy diskette
Data Capacity	320K bytes formatted
Number of tracks	70 (35 per side)
Track density	48 TPI
Rotational speed	300 rpm
Start/Stop time	.5 sec
Average latency	100 ms
Head Load time	35 ms
Access time	5 ms track to track
Data transfer rate	250K bits/sec.
Dimensions	3.5 in. X 5.75 in. X 7.5 in. (8.255 cm. X 14.605 cm. X 19.05 cm)
Weight	3.0 lbs. (1.36 Kg)

MECHANICAL AND ELECTRICAL SPECIFICATIONS

PARAMETER	CHARACTERISTICS
Media	ANSI standard 5 1/4-inch diskette
Number of Tracks	40/51 70/52
Track Density	48 TPI
Start/Stop Time	0.5 sec
Rotational Speed	300 rpm $\pm$ 1 1/2%
Average Latency	100 msec
Head loading time	35 msec
Access time	5 msec, track-to-track
Head settling time	15 msec
Access time	15 msec
Head life	20,000 hours
Media life	3×10^6 passes on single track
Recording method	FM, MFM, M^2FM
Recording density (FM)	2810/5620 bpi
Flux density	5620 fci max.
Data-transfer rate	125K/250K bits/sec.
Power-up Delay	0.5 sec
Height	3.25 inches (8.255 cm)
Width	5.75 inches (14.605 cm)
Length	7.5 inches (19.05 cm)
Weight	3.0 pounds (1.36 kg)
Power	+12 VDC $\pm$ 5%, 0.8A (1.5A surge)
	+5 VDC $\pm$ 5%, 0.4A
Typical Power Dissipation	12W Operatin
	6W Standby
Operating Temperature	$40^\circ F$ to $115^\circ F$ ($4.4^\circ C$ to $46.1^\circ C$)
Storage Temperature	$-40^\circ F$ to $160^\circ F$ ($-40^\circ C$ to $70^\circ C$)
Operating Humidity	20% to 80% (noncondensing)
Storage Humidity	5% to 95% (noncondensing)
Operating altitude	-500 ft to 10,000 ft (-152.4m to 3,048m)
Storage altitude	-1000 ft to 50,000 ft (-304.8m to 15,240m)
Vibration and Shock (Operating)	6 to 600 Hz, 0.5g

CHAPTER 2
INSTALLATION

The installation instructions contained herein cover operational site requirements, and preparation of the equipment through initial operational checkout.

2.1 SITE PREPARATION

1. Be sure the correct power input is available at the recommended site, 115Vac (+10, -15%) at 60Hz or 230Vac (+10, -15%) at 50Hz.

2. The main power cable requires a grounded three prong plug.

3. There are three cable lengths to consider for placement of the system. They are as follows:

Keyboard-to-Terminal	10 feet
Terminal-to-Printer	10 feet
Main Power Cord	8 feet

4. The monitor is a desk-top ergonomic model. Choose an adequate piece of furniture (see specification in Chapter 1).

5. It is suggested that the floor-standing printer console be positioned to the right of the monitor. This arrangement allows the operator convenient access to the diskette drive, printer control panel, and ON/OFF switch.

2.2 ENVIRONMENTAL CONSIDERATIONS

The recommended temperature for the equipment is 15°C to 28°C (60°F to 80°F). Temperature control is an important factor because the Wangwriter is cooled by the surrounding room air. If the system is to be situated in direct sunlight, there should be a shading device available to eliminate the excessive heat.

The recommended relative humidity should be maintained between 40%-60%.

Ideally, the storage environment for the diskettes should be the same as the system environment since extremes of either heat or humidity may adversely affect diskette reliability.

Normal precaution should be taken to keep dust, dirt, and other foreign matter away from the equipment. The amount of contamination typically found in the air in a normal business environment will not interfere with the operation of the equipment.

. Static electricity may interfere with operation of the equipment. It can be minimized or eliminated either by avoidance of installing equipment in a carpeted area or by treatment of the carpet with anti-static sprays. Additionally, selection of furniture with anti-static unholstery and metal wheels, and maintenance of room humidity at about 40% (particularly during winter months) may help.

The power, heat dissipation and physical dimensions are given below:

ERGO CRT TERMINAL

Total Dimensions	Inches	Centimeters
Height	15.0	38.1
Depth	12.8	32.5
Width	13.5	34.3
Net Weight	Pounds	Kilograms
	28	12.72

PRINTER CONSOLE

Total Dimensions	Inches	Centimeters
Height	26.8	68.1
Depth	12.0	30.5
Width	22.0	55.9
Net Weight	Pounds	Kilograms
	73	33.18

SYSTEM POWER INPUT
AND HEAT DISSIPATION

Power Requirements	115/60Hz	230/50Hz
Amps	4	2
Watts	300	
Dedicated Line	No	
Heat Output (Max)	BTU/HR	KCAL/HR
	1020	0.257

Cable Length (Max)	Feet	Meters
Console to CRT Terminal	10.0	3.0
Console to Keyboard	10.0	3.0
Console to Power Source	8.0	1.83

2.3 UNPACKING

The Model 5503 Wangwriter system is packaged in three separate containers containing respectively the printer console, keyboard and CRT terminal.

The keyboard is shipped in a carton large enough to include the following items packaged in protective enclosures:

1) One 10 ft 4-wire keyboard signal cable attached to the keyboard
2) Two (2) floppy diskettes (5 1/4 inch size)
3) One ribbon cartridge
4) One daisy printwheel
5) System ac power cord
6) Installation and instruction manual(s)

The printer unit is shipped on a wood pallet with a cardboard box strapped over it. Cardboard or foam protection is provided at the top of the box. The unit is removed by the cutting of the straps, the box lifted up over the top of the printer and the printer lifted off the pallet.

The CRT is protected in its carton with foam blocks on each corner. A dual video/power cable is attached to the CRT unit.

2.4 SYSTEM INTERCONNECTIONS

After unpacking the system, place system units in their planned locations and perform the following interconnections.

1. Connect the 10-ft four-wire cable attached to the keyboard to the CPU connector on back of the printer console. The connector has a flat side for pin alignment and needs only to be pushed into the lock position.

2. Connect the 10-ft dual cable/connectors between the CRT and printer console. The (BNC) connection is on the rear connector panel of the printer console; the other cable connects to the connector on the power supply.

3. Connect the 8-ft ac power cable between printer console (bottom-rear) to the designated power output receptical.

2.5 INSPECTION

Chapter 7, Replacement and Removal contains the procedures to gain access to the interior of the three units. Refer to these procedures, if necessary, during the inspection procedures.

1. Make sure all connectors are plugged in as listed: (see Figure 2-1).

	Location	Connector	Name
7776* Printer PCA	Outside of card cage	J2	Printwheel motor/ribbon motor
		J3	Power supply
		J4	Carriage motor
		J5	Paper Motor
		J6	Sensors
		J7	Switch panel
7777 CPU	Middle of card cage	J2	Disk 0
		J3	Disk 1 (not used normally, an option.)
		J4	Keyboard
		J5	Power supply
7775 CRT/MEMORY	Inside of card cage	J2	Video monitor (BNC)
P.S. 7778 Regulator	Power Supply drawer	J1	To power supply
		J2	To CPU PCA
		J3	To printer PCA
		J4	To disk drive 0
		J5	To disk drive 1 (Option)
		J6	To CRT terminal

* The printer PCA must be positioned on the outside to ensure adequate cooling under normal operation.

2. Check the SW1 8-position option switch on the CPU PCA. The switches should be positioned as shown below for normal operation: (The switch is located near the lower right-hand corner of the PCA.)

	1	2	3	4	5	6	7	8	Switch Numbers
ON	●	●	o	o	o	o	o	o	SW1
OFF	o	o	o	o	o	o	o	o	CPU PCA

PUT S4 ON FOR DUAL DISK DRIVE

NOTE

The printer board must be removed to check the switch positions. Handle all connectors carefully and be sure you will know which connector mates to which PCA terminals. The procedures to remove the Printer PCAs are given in Chapter 7.

CAUTION

Be sure all ZIF connectors are seated properly.

3. Install all PCAs in their recommended position in the card cage and mate all connectors.

NOTE

Do not put the side cover on at this time.

4. Remove the shipping dummy diskette from the disk drive.

2.6 INITIAL TURN ON/POWER UP DIAGNOSTIC

CAUTION

BE SURE THE SHIPPING DISKETTE (DUMMY)
IS REMOVED FROM THE DISK DRIVE.

1. Press "1" on the red power switch to turn system ON.

NOTE

Normally the system will automatically perform the power-up diagnostic. Also, the system will normally hang-up on test #9 indicating a disk fault because a disk has not been inserted. However, continue with procedure steps 2, 3, 4, 5, 6, 7, etc.

Should the system not respond (fan not running) check the fuse on the back panel of the printer console and check that the power plug is properly inserted in its outlet. If OK, replace both the regulator board and the power supply if necessary. See Chapter 7 for replacement and removal. Restart system (procedure 1).

2. Open the diskette drive door by pulling the door flap back toward the left side of the console.

3. Remove the starter/utility diskette from its paper dust jacket.

4. Be sure the write protect slot is not covered with a tab.

NOTE

The protective shield is labled with arrows indicating the proper direction for inserting the mini-diskette. If your diskette does not have arrows, refer to Chapter 3 for instructions.

5. Gently push the mini-diskette into the drive slot until it catches in place.

6. Close the diskette drive door until it locks in place. The door must be kept closed.

NOTE

Once the starter/utility disk has been properly inserted, the system will load and display the menu of the starter/utility diskette if the system has passed the power-up diagnostic.

7. Should the system hang-up during the power-up diagnostic sequence because of a fault, check the various power supply voltages at the following specified locations:

VOLTAGE	LOCATION
+5V (4.75 -to- 5.25Vdc)	J1 Printer PCA pin 1, ground pin 3
+12V (11.40 -to- 12.60Vdc)	J1 Printer PCA pin 5, ground pin 3
-5V (-4.75 -to- -5.10Vdc)	J1 Printer PCA pin 7, ground pin 3
-12V (-11.76 -to- -12.24Vdc)	J1 Printer PCA pin 9, ground pin 3
+18V (+14.00 -to- 21.00Vdc)	J3 Printer PCA pin 1, ground pin 3
+36V (+28.00 -to- 42.00Vdc)	J3 Printer PCA pin 5, ground pin 3

NOTE

If all voltages are satisfactory perform steps 8 through 10. If not within specified limits, perform steps 11, 12, 13. If +18V is not present, first check (and if blown) replace the fuse (F2) on the power supply (regulator board).

8. Should all the voltages be satisfactory, turn the system off by pushing 0 on the red power switch.

9. After 15 seconds, turn on the power by depressing 1 on the red power switch.

10. Should the power-up sequence hang-up because of a fault re-seat power and signal connectors and if fault still persists replace the PCA specified in the following chart: the chart identifies the logic being tested, the fault indication on the 7 segment LED (visable from the back of the unit near the connector) and the PCA on which the failure has occured.

NOTE

If system passes power-up diagnostic after PCA replacement, begin normal operation procedures after putting on side covers. If system is not operating normally, see the fault analysis in the maintenance chapter.

ERROR CODE	PCA		FRU
.8	CPU	7777	Z80 (.8 = the power-up value of the 7 - segment display.)
0	CRT/MEM	7775	VTAC
1	CRT/MEM	7775	MAIN MEMORY
2	CRT/MEM	7775	CRT MEMORY
4	CPU	7777	PROM
5	CPU	7777	DATA BUS (Not an FRU)
6	CPU	7777	FDC (floppy disk controller)
7	CPU	7777	CPU UART OR PIO, KEYBOARD CABLE, KEYBOARD UART
9	CPU	7777	CTC
A	CPU	7777	FDC, DISK DRIVE, OR DISK DRIVE CABLE
E	PRINTER	77776	PIO

11. Should any of the 5 and 12V voltages be out of specifications, adjust the +5VR and on the +12VR by potentiometer R2 and R1 respectively. They are located on the regulator board of the power supply. See Chapter 5 for adjustment.

12. Should any of the voltages be out-of-specification after adjustment, replace regulator board and then the whole power supply, if necessary (see replacement procedures in Chapter 7).

13. After replacement, if problem still persists, see fault analysis in the diagnostics chapter (Chapter 6) of this document.

14. For a checkout of proper operation of the printer, see paragraph 6.1 of this manual.

CHAPTER 3
OPERATION

The performance of various operational procedures is requisite for Wangwriter servicing. Applicable procedures include those necessary for observation of equipment operation; the steps contained herein enable such observation via either audio/visual means or system diagnostics.

3.1 INITIATING SYSTEM OPERATION

The activating of the installed system involves the insertion of a minidiskette (excepting those instances in which a PROM-based routine is used, see Disk Alignment - Chapter 5) and the application of power The type of operation desired (i.e., either word processing or running of a system diagnostic routine) determines which minidiskette is to be used. The following steps apply to either type of operation.

1. Pull diskette-drive door open.
2. Remove paper dust jacket from the mini-diskette (do not remove permanent protective shield).

NOTE

The write/protect slot on the system or diagnostic (read only) mini-diskette should be uncovered.

3. Insert minidiskette, as indicated by arrows on the package into the minidiskette drive until the minidiskette clicks into place.

4. Close the diskette drive by pushing the door latch to the right until it clicks.

5. Press the 1 on the on/off switch. The POWER indicator should illuminate, and following a 30-second interval an instructional/informational display (menu) should appear on the monitor. (For either operational or system diagnostic menu descriptions, refer to respective coverages: Wangwriter Reference Manual or System Diagnostics, Chapter 6 in this manual.)

6. Remove system minidiskette and replace in the paper dust jacket (Word processing system minidiskette only. See System Diagnostic for disposition of diagnostic minidiskette).

Should the monitor fail to display a menu, either a system fault or an improper insertion of the minidiskette (or a faulty minidiskette) may be indicated. In such an instance, a reinsertion (with a different system minidiskette, if necessary) should be attempted. Should any letter or number other than an inverted letter A appear in the 7-segment display on the back of the priter console, the error code may isolate the fault to a general area as shown in the following table.

ERROR CODE	PCA		FRU
.8	CPU	7777	Z80 (.8 = the power-up value of the 7 - segment display.)
0	CRT/MEM	7775	VTAC
1	CRT/MEM	7775	MAIN MEMORY
2	CRT/MEM	7775	CRT MEMORY
4	CPU	7777	PROM
5	CPU	7777	DATA BUS (Not an FRU)
6	CPU	7777	FDC (floppy disk controller)
7	CPU	7777	CPU UART OR PIO, KEYBOARD CABLE, KEYBOARD UART
9	CPU	7777	CTC
A	CPU	7777	FDC, DISK DRIVE, OR DISK DRIVE CABLE
E	PRINTER	77776	PIO

Should a minidiskette for storing documentation (archive diskette) instead of a system diskette be inserted accidentally, a message "Wrong Disk" appears on the monitor. A switch to the proper minidiskette and recycle of power-up should restore proper operation.

3.2 INSERTING AN ARCHIVE MINIDISKETTE

The insertion of an archive minidiskette follows generation of a start-up menu as described in paragraph 3.1. To insert the archive mini-diskette:

1. Remove paper dust jacket from the minidiskette (do not remove permanent protective shield).

   NOTE

   The write/protect slot on the archive mini-diskette should be covered to permit writing by the system.

2. Insert minidiskette (the minidiskette should be oriented with the write/protect slot at lower edge).

3. Actuate space bar to move cursor to desired option of start-up menu.

4. Press EXECUTE. A prompt, "Press EXECUTE when archive disk is in drive" should appear in the message line. Press EXECUTE again; the message should disappear, and the selected activity menu (or prompt) should display. (See Wangwriter Reference Manual for instructions on specific activity options.) Should the archive minidiskette be either absent or improperly inserted, a prompt, "Drive not ready," appears in the message line. In such an instance, (re)insert minidiskette, and press EXECUTE.

The archive diskette must remain inserted in the drive throughout the word-processing operation. The red indicator, illuminated, indicates that the drive is locked with an archive minidiskette in place. The drive cannot be opened until the "Remove Archive Disk" option on the start-up menu has been selected. At this selection, the red indicator light goes dark and a prompt "Remove Disk" appears in the message line.

3.3 SYSTEM RESET

A system reset, comprising either a deselection of an activity option or a complete power turn-off, may clear a malfunction caused by a transient condition such as:

- Low power, or power failure
- Static electricity
- Incorrect insertion of the system minidiskette

To clear such a temporary condition:

1. If the malfunction occurs during initial start-up, check that the system minidiskette is inserted properly (see paragraph 3.1).

2. If the malfunction occurs when text is on the screen, try to return to the start-up menu by pressing CANCEL and EXECUTE. If not successful, proceed to step 3. If successful, position the cursor at "Remove Archive Disk" and press EXECUTE.

3. Turn the system off by pressing 0 on the on/off switch.

4. Remove the minidiskette from the drive.

3.4 PRINTER OPTION

The procedure for initiating a start-up menu, paragraphs 3.1 and 3.2 should procede the following steps.

1. Make sure that the printer is deselected. If the red indicator at the SELECT switch is glowing, press SELECT. The indicator should go dark.

2. Via the space bar, position the cursor at "Print Document" on the start-up menu, and press EXECUTE. A prompt, "Enter Document Name" should appear on the display.

3. Enter the eight-character code representing the desired document and press EXECUTE. The Print Document menu should appear on the screen.

4. Press RETURN key to move cursor to various fields in the Print Document menu. Make changes by typing over existing entries. When desired changes (if any) have been made, press EXECUTE. The start-up menu shold reappear and the CHANGE PAPER indicator should glow.

5. Insert paper in the printer by pulling the paper loading lever forward. Be sure that the paper is aligned with the left-most edge of the paper guide.

6. Adjust page to the desired starting line position via the LINE FEED or ROLL up/down switches on the printer control panel.

7. Select printer by pressing SELECT switch. The printer should begin printing. The printer automatically ejects each finished page either up or down as indicated in the Print Document Menu.

8. For each additional page to be printed, deselect printer via SELECT switch, and insert new paper. Press SELECT switch.

9. To terminate the print activity, access the "Cancel Print Request" activity on the Special Print Functions menu.

CHAPTER 4

THEORY OF OPERATION

The Wangwriter Model 5503 is a "stand-alone" word processor consisting of three separate units: an "ergonomic" display unit, a remote keyboard unit, and a floor-standing cabinet housing a daisy printer, a mini floppy, three Wang logic PCAs and a power supply/regulator which provides power to all system units. The display unit and keyboard may be positioned independently for ease of operation. See Figure 4-1 for a simplified block diagram.

The mini floppy-disk drive located in the printer cabinet, is a double-sided, double-density, diskette with a capacity of 300,000 bytes.

96K of RAM main memory (on the CRT/MEM PCA) is used to store the operating system software, character set, etc. It is also used as a buffer between CRT memory and disk, and between keyboard and CRT memory for example. Because all software is in the system RAM, an archive diskette is used solely as a storage medium for text. There are no DMA paths. All data transfers are handled by the Z80A CPU.

Printing is done in the background mode and the actual output speed is an average 20 characters per second (bidirectional).

As seen in Figure 4-1, the three PCAs in the floor-standing cabinet are: CPU, CRT/MEM, and Printer PCA. The CPU PCA contains the Z80A CPU, bootstrap and power-up diagnostic PROM and a UART* for converting keyboard serial data to parallel. It also contains a PIOA, for controlling keyboard and disk information to and from the Z80A-CPU and a CTCA* chip which principally provides timing of phase changes for the stepping motors in the printer. It is also used as a general system real time clock. A UPD765* chip provides a LSI interface between the minifloppy disk and the Z80A CPU environment.

*See Appendices for detailed operation.

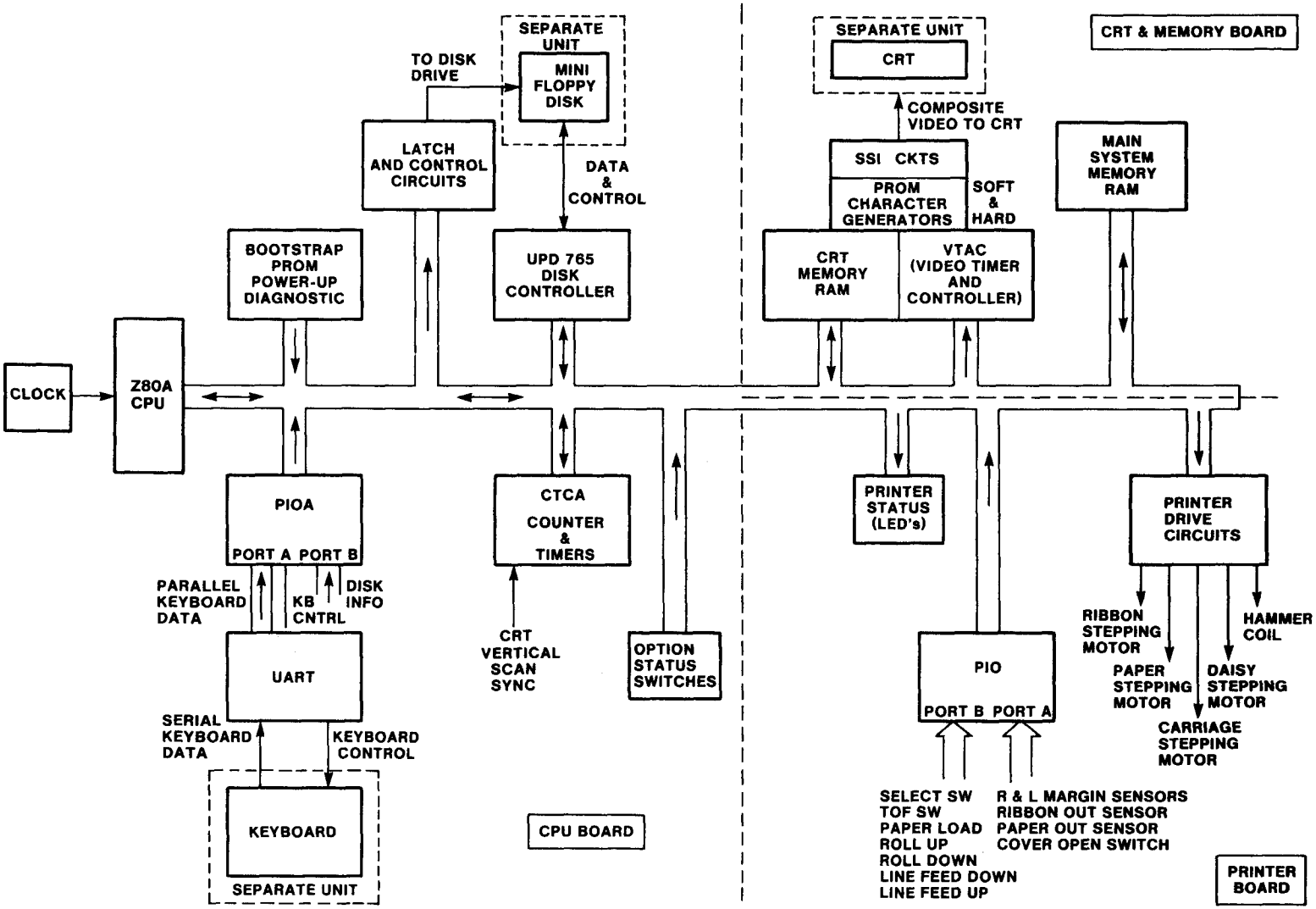


FIGURE 4-1 SIMPLIFIED SYSTEM BLOCK DIAGRAM

The CRT/MEM PCA includes the 96-K byte system operating Ram Memory into which the operating system program is load from the starter/utility disk each system start-up. The PCA also contains a 5027 VTAC* (Video Timing and Counter) chip which provides the main interface between the CRT and the CRT memory. Both a soft (programmable) and a hard character generator are provided by RAM and PROM chips respectively.

The printer PCA has its own PIO chip which controls to the Z80A CPU data and the status of the printer through both A and B ports. The PCA also contains printer- driver circuits for the four motor circuits: ribbon, paper, carriage and daisy or print wheel. A digital drive circuit is also provided to actuate a hammer that forces the petal of the daisy print wheel onto the ribbon which prints on the paper.

The Z80A CPU, of course, is the heart of the CPU PCA and the system. As programmed, it will monitor the status of the various input ports and provide up-dated information to the output ports. It does this through its three main busses: address, data, and control. Because all the input/output devices are tied to a common bidirectional data bus, while the Z80A CPU is communicating with one port, it causes all the other ports to present a high impedance to the bus so there is no interference. The details on how the Z80A functions is provided in Wang's Z80 reprint 03-0002-00.

The ergonomic display monitor houses one CRT Electronics PC board (7456) which contains standard CRT input video and scanning circuits. The operation of this board is contained in Service Bulletin #73. The floppy disk also has a printed-circuit assembly. The functional operation of this board is contained in MPI's Flexible Disk Drive, Model 51/52, Product Manual (Revision 3).

The keyboard also contains a PCA. It provides serial keyboard character and control signals to the system's CPU PCA. The major circuits are: a capacitive keyboard, an encoder, a unique multiplexer and a UART for parallel to serial data conversion.

*See Appendices for detail operation.

The following functional discussion will make reference to Figure 4-13, the system functional block diagram. Several more functional drawings are used to amplify certain areas. We will begin with the functional operation of the system clock. The Z80A microprocessor, system turn-on and power-up diagnostics, system RAM operating memory, floppy disk communications, CRT display and logic, printing communications, keyboard communications and system interrupt follow the clock's discussion.

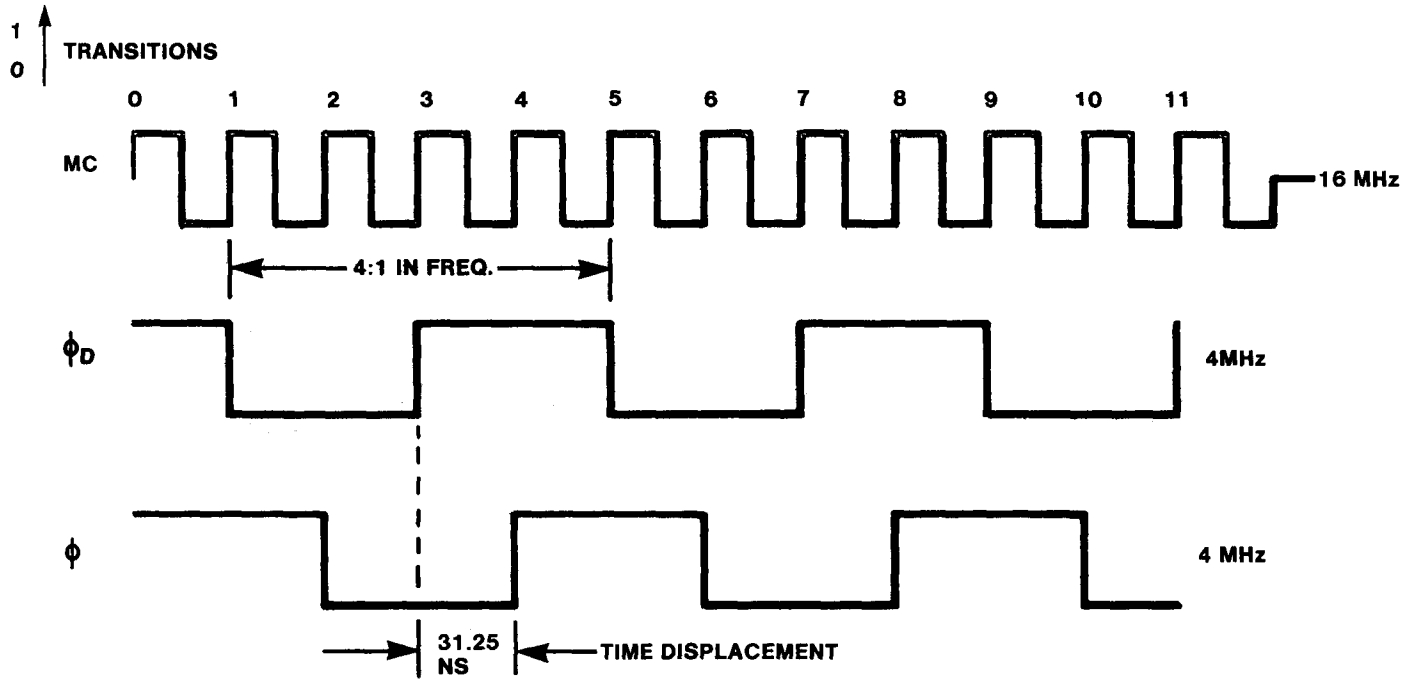


FIGURE 4-2 CLOCK OUTPUT

4.2 Z80A MICROPROCESSOR

The Z80A-CPU microprocessor chip, coupled with the electronically loaded system RAM memory, is essentially a complete CPU for the system. As indicated in the system functional block diagram (Figure 4-13), the Z80A-CPU uses an exterior 8-bit bidirectional data bus for data transfer and a 16-bit unidirectional bus for addressing the various memories and I/O ports. The Z80A-CPU performs these and all other functions by stepping through a few basic operations at high speeds; such as internal data processing, data transfers, memory read and write, and I/O device read or write. Through the use of specific addresses, Z80A-CPU buffered control signals, and the output of decoders, the various memories and I/O ports can be addressed and enabled. Clocking is provided by either one of the three clock signals.

The Z80A CPU obtains its precise programmed operating instructions by addressing the electronically loaded (loaded from the starter/utility diskette) RAM system operating memory on the CRT/MEM PCA. As the Z80A-CPU processes the instructions, it is effectively told to read from or write to memories and input/output device data. To perform these various commands, the Z80A-CPU listens to or talks to the various system devices; such as printer, floppy disk, display unit and keyboard. The sequence of communication with the various I/O ports and memories is determined by the system program. The Z80 Wang reprint (#03-0002-00) will provide information regarding the detail workings of the microprocessor chip.

4.3 SYSTEM TURN-ON AND POWER-UP DIAGNOSTICS

As soon as power is turned-on by the red front-mounted power switch, on the front of the printer's cabinet, POR (power on reset) is developed by an RC network and inverters (see Figure 4-3). POR has two major functions, one is to reset the CPU to the beginning of its program (0000) and the other is to reset all circuits such as flip-flops to a known reset state.

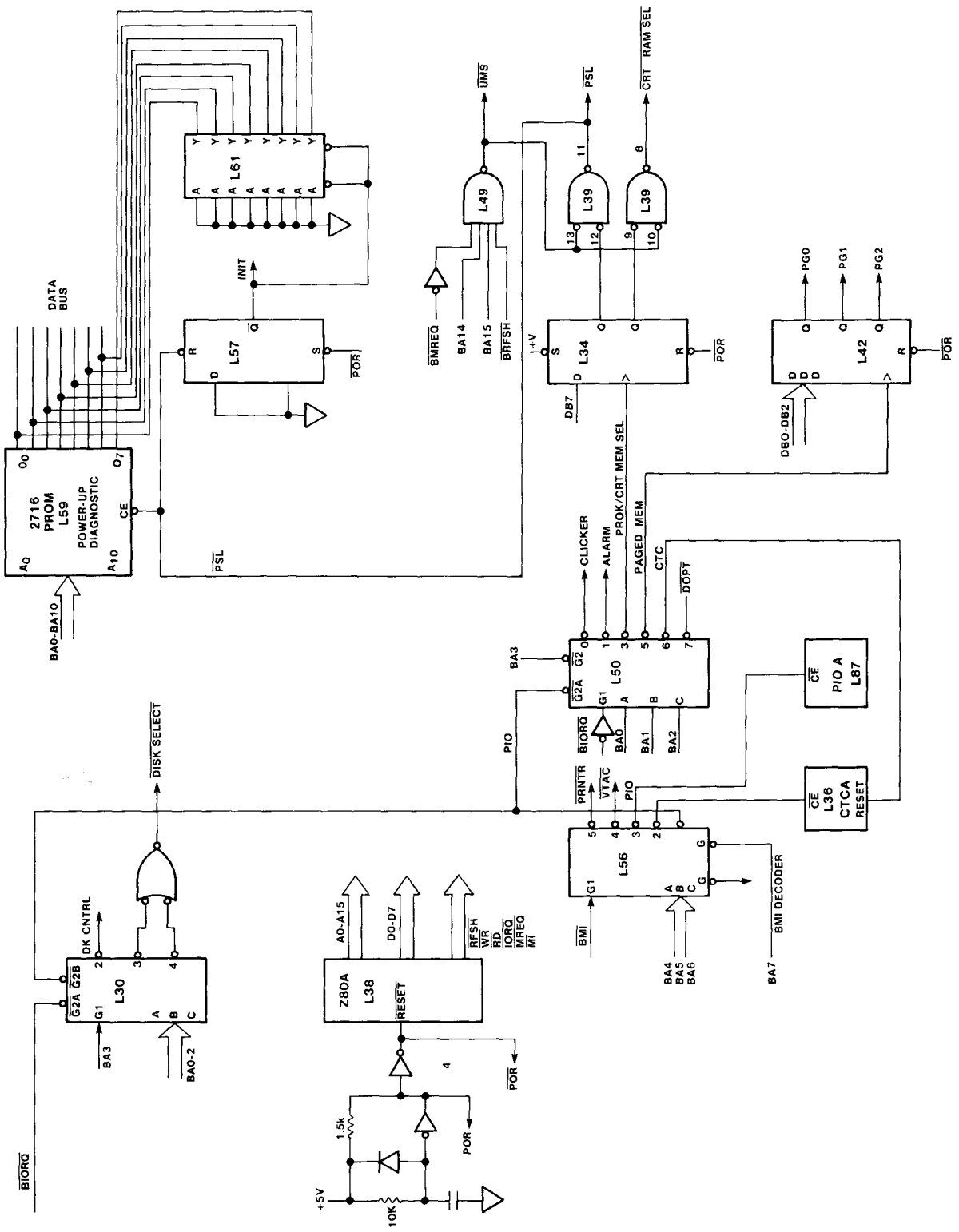


FIGURE 4-3 POWER-UP RESET LOGIC

It should be also noted that the software must go through the following sequence during initialization to allow the real time clock to start properly:

1) Initialize VTAC
2) Initialize CTC ch 2
3) Disable CTC reset (Control Register D3=1)
4) Enable CPU Interrupts

The power up diagnostic will determine, 90% of the time, the location of a malfunction to a particular PCA and is run during every start-up time. (The power-up diagnostic is explained in more detail in the maintenance section of this manual.)

As the Z80A microprocessor cycles through addresses 0000 to C000, NO-OP commands are performed to permit signal settling. During this time, the DB0 through DB7 data bus signal lines are inhibited through buffer L61 by grounding the bus. (See Figure 4-3 the memory and device addressing/-selection circuits). Also see memory and I/O addresses in Appendices F and G, and see Figure 4-13 for overall system aspects.

During all active PROM addresses (C000 through C3FF), the buffer L61 becomes a high impedance (removing data bus grounding). The PSL (PROM Select Latch) signal becomes low at address C000 activating the power-up diagnostic and bootstrap PROM. PROM access will occur when BA4 through BA7 are low, and BM1 high (at L56), providing a low (port 0) to the input/output decoder (L50). This enables the input/output decoder when its BA0 through BA2 inputs become H, H and L respectively. The decoder will provide a low output at port 3 during BIORQ time.

The low output from port 3 of input/output decoder (L50) clocks the low input (DB7) at L34-2 to the Q output and latches it to a low level (DB7=0). This low combined with UMS (upper memory select) low provides a low to the CE (chip enable) input of the PROM through the positive OR gate L39-11. A low PSL also resets FF (L57, INIT signal) to remove the grounds on the data bus. This allows the Z80A CPU to receive preprogrammed instructions and data from the PROM as it is addressed from C000 through C3FF.

It should be noted that BA3 and BA7 are inputs to L50 and L56 decoders respectively. When these signals are high, all the outputs of the decoders become high.

During initial PROM activation, the power-up diagnostic will be run checking the systems major components. The components and fault indications are as follows: (The PCA on which the component is located is also indicated.)

ERROR CODE	PCA		FRU
.8	CPU	7777	Z80 (.8 = the power-up value of the 7 - segment display.)
0	CRT/MEM	7775	VTAC
1	CRT/MEM	7775	MAIN MEMORY
2	CRT/MEM	7775	CRT MEMORY
4	CPU	7777	PROM
5	CPU	7777	DATA BUS (Not an FRU)
6	CPU	7777	FDC (floppy disk controller)
7	CPU	7777	CPU UART OR PIO, KEYBOARD CABLE, KEYBOARD UART
9	CPU	7777	CTC
A	CPU	7777	FDC, DISK DRIVE, OR DISK DRIVE CABLE
E	PRINTER	77776	PIO

Error indications appear on a seven-segment LED display. The LED readout is located on the rear of the printer's stand.

Once this routine is run without error, the PROM bootstrap will load the operating system program into the system's 96k byte RAM memory from disk. From this point on, the system RAM memory on the CRT/MEM board will provide Z80A-CPU microprocessor with instructions and data.

4.4 SYSTEM RAM OPERATING MEMORY

The system program operating RAM memory is located on the CRT/MEMORY PCA and when electrically loaded from the starter/utility floppy, contains the system operating program. It also serves as a buffer memory for the CRT memory and the floppy disk and the keyboard. The memory is dynamic and is refreshed by BRFSH from the Z80A-CPU microprocessor buffers.

There are six banks of eight 4116 RAM dynamic memory chips on the CRT/MEMORY PCA. Therefore, chip loading results in an 96-K byte RAM memory.

The memory addresses are as follows:

0000-3FFF -- bank 1
4000-7FFF -- bank 2
8000-BFFF -- Paged memory

The four banks of paged memory are selected by data bits D0 and D1 and an "OUT 05" Opcode as indicated below.

BIORQ decoder	OUT05,	D0=0, D1=0	Page 0 -- bank 3
		D0=1, D1=0	Page 1 -- bank 4
		D0=0, D1=1	Page 2 -- bank 5
		D0=1, D1=1	Page 3 -- bank 6

See Appendix G for additional information memory and I/O addressing.

4.4.1 RAM Address Decoding

The Z80A-CPU buffered address signals (BA0 through BA13) are multiplexed (L78, L46) as A0 through A6 and A7 through A13 into all the 4116 RAM memory chips on the PCA. These 14 address bits are required to decode to 1 location in one of the 4116 chips (see Figure 4-13).

RAS (row address strobe) latches the seven-row address bits into the 4116 chips and the CAS (column address strobe) subsequently latches in the seven-column address bits. The combination gives an address capability of 16K.

Memory banks 1 and 2 are selected by one half of the L115 multiplexer (see Figure 4-13). Its inputs are BA14 and BA15. Both BA14 and BA15 are low for addresses 0000-3FFF hex. BA14 is high and BA15 is low from address 4000-7FFF. When BA is low and BA15 is high from (8000-BFFF), PG0 and PG1 codes select banks 3 through 6 (4000-BFFF).

NOTE

D0=0, D1=0 ---- page 0 --- Bank 3

D0=1, D1=0 ---- page 1 --- Bank 4

D0=0, D1=1 ---- page 2 --- Bank 5

D0=1, D1=1 ---- page 3 --- Bank 6

Data bits DB0 and DB1 from the Z80A-CPU set up the correct PG codes (see Figure 4-3). These actions essentially select the active memory chip (paged memory) and cell by activating a given RAS or PRAS signal. (All the CAS strobes are activated simultaneously after the RAS/PRAS strobe.)

To select bank three for example (see Figures 4-3 and 4-13). The Z80A-CPU would be sending a low order address code 101 (A0, A1, and A2 respectively) while BIORQ is negative which drives L50-5 low. On the rise of the clock, FF L42 develops a low for both PG0 and PG1, selecting bank three as shown in Figure 4-13.

The 74S194 (L95) shift register (see Figure 4-13) determines the timing required between activation of row address and column address select (RAS/PRAS and CAS) as shown in Figure 4-4 timing diagram. The fetch instruction shown below is a typical read function of the Z80A.

4.4.2 Fetch Instruction

L94, L93, and L95 are the major logic between the Z80A-CPU and the system RAM memory (see Figure 4-13). They set up the the memory for fetch, read, and write operations for example. Figure 4-4, RAS, PRAS and CAS strobing times, shows the timing of the logic during a fetch instruction operation.

As the L93 NAND gate goes low and MC clocks the L95 shift register (with S0 high and S1 low), the shift register L95 outputs a low on QA through QD. The next MC pulse clocks a high on QA output. (Because SR is high and SL is low, the pulse shift is right.) The next MC pulse causes QB to go high, etc.

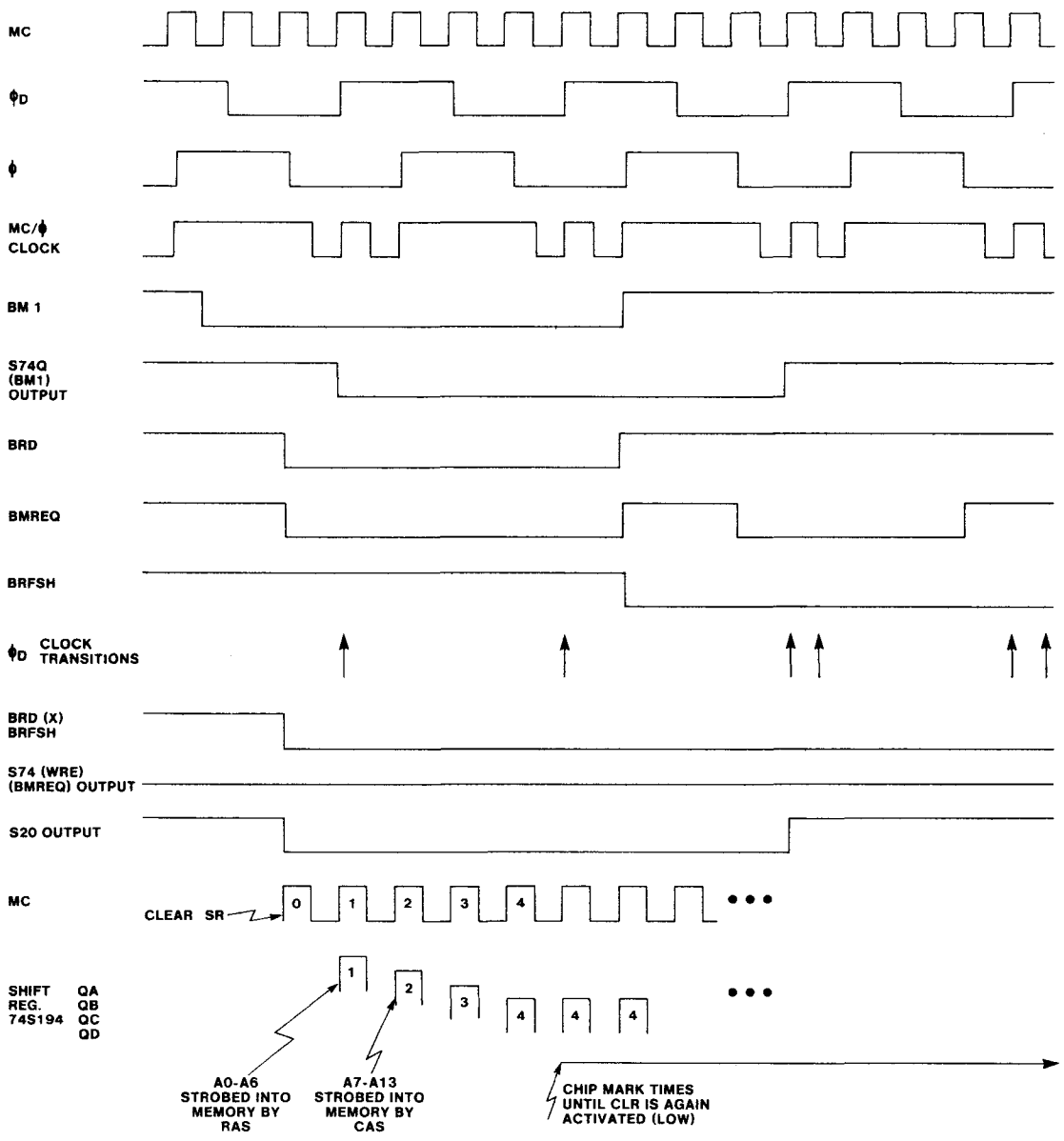


FIGURE 4-4 RAS, PRAS AND CAS STROBE TIMES

QA high allows RAS/PRAS (X) to data strobe into the RAM memory with address bits A0 through A6 via L78 and L46 multiplexers. When QB becomes high on the next MC pulse, the CAS strobes A7 through A13 address bits through the same multiplexers. Both of these addresses are latched in the 4116 chip logic and activates a single memory location.

QB also enables L112 when it is high. At this time, the D inputs (memory data) are latched on the Q outputs. Because WRE, UMS, BIORQ, and INIT are all high, L109 output becomes low and directly allows the output OC of L112 on the data bus (data read). With this action, the Z80A-CPU receives its instruction information.

4.4.3 Main Memory Write

The system operating memory, due to timing considerations, uses the early-write cycle mode (WRE active before CAS goes active). When WRE of system memory goes low, the input to OC of the L112 goes high, presenting a high impedance to the bus (see Figure 4-13). With WRE (pin 3 on chip) activated and the LS244 (L111) input port activated (always activated), the Z80A-CPU will be able to write data into the memory at the location established by the address information from the Z80A. CAS negative transistion will strobe the data into the memory.

4.4.4 Refresh Memory

Refresh of the dynamic cell matrix or memory location is accomplished by performing a RAS memory cycle at each of the 128 row addresses within each 2 millisecond time interval. This function is accomplished at RAS/PRAS cycles to minimize power consumption.

The Z80A-CPU output RFSH active low indicates that the lower 7 bits of the address bus contains a refresh address for dynamic memories and the current MREQ signal is used to do a refresh read (the output port is open).

4.4.5 TC Option

PG2 via page latch (DB2) will be used to disable the four paged main memory banks and enable TC memory on the TC PCA when the TC option is included in the system. TC will be available in future systems.

4.5 FLOPPY DISK COMMUNICATIONS

The 5503 system uses a flexible disk drive, MPI Model 52, to store documents and load the operating system information into the system operating RAM on the CRT/MEM PCA. Communications are only between the floppy and the Z80A-CPU microprocessor. Unformatted data capacity is 6.25K bytes for one track and 437.5 for the double density disk using MFM recording. See Micro Peripherals, Inc. instruction manual revision 3 for floppy details.

4.5.1 Overview of Floppy

The floppy drive is self-contained and requires no operator intervention during operation. The drive consists of a media-rotating system, a head-load and positioning system, and a write/erase and read system (see Figure 4-5a.) When the front door is opened, access for inserting the diskette is provided. When inserting the diskette, all positions except in/out are controlled by physical guides internally. Correct in/out is assured by inserting the diskette until a "click" is heard. Closing the front door activates the cone/clutch system which serves two purposes in the following order:

1) Correct centering of the media.
2) Clamping the media to the spindle hub.

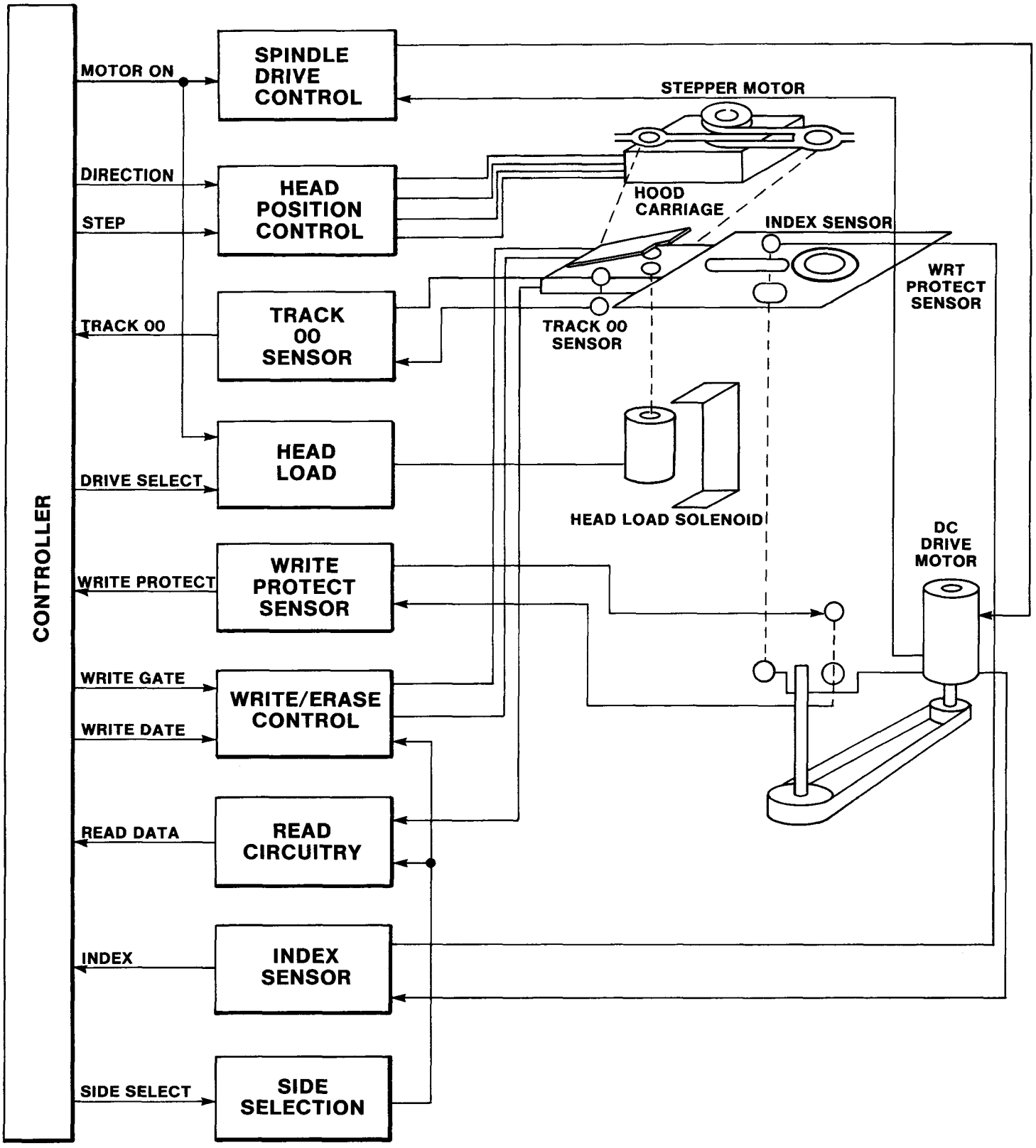


FIGURE 4-5(A) FLOPPY DISK FUNCTIONAL BLOCK DIAGRAM

The spindle hub rotates at a constant speed of 300 rpm by means of a dc motor/tachometer and a reference in a closed-loop system. When in operation, it is important that the head-to-media relationship be controlled. This is accomplished by the head-load system in the following way: The media is pressed against a reference platen which is referenced to the head and the spindle hub; and a pressure head is loaded against the media on the opposite side of that head with a force of approximately 17 gr. The recording heads are positioned over the correct track by means of a four-phase stepper motor/band direct-drive mechanism, and its associated electronics. A one-step movement causes a one-track movement. With band positioning, very high step rates can be accomplished with the 52 system. When a Write Protected diskette is inserted, the write protect sensor disables the write/erase circuits in the drive. When writing, a 0.013 inches (nominal) data track is recorded, followed by a tunnel erase which trims the track down to 0.12 inches (nominal). Data recovery electronics include a low-frequency amplifier, a differentiator, a cross-over detector, a digital filter, and a final pulse generator. A data decoder separates clock and data pulses on the I/O connector. See MPI's Flexible Disk Drive, Model 51/52, Product Manual (Revision 3).

4.5.2 Overview of Floppy Disk Controller (FDC)

A UPD765 Floppy Disk Controller (FDC) is used as the interface between the Z80A-CPU and the floppy disk. The chip is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. It is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC (floppy disk controller) receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

During command or result phases, the status register of UPD765 (see Figure 4-5b) must be read by the processor before each byte of information is written into or read from its data register. Bits D6 and D7 in the status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the UPD765. On the other hand, during the result phase, D6 and D7 in its status register must both be 1s (D6=1 and D7=1) before reading each byte from the data register. Note, however, this reading of the status register before each byte transfer to the UPD765 is required in only the command and result phases, and NOT during the execution phases.

During the execution phase, the main status register need not be read. If the UPD765 is in the NON-DMA mode, then the receipt of each data byte (if UPD765 is reading data from FDD, floppy disk drive) is indicated by an interrupt signal (INT=1). The generation of a read signal (RD=0) will reset the interrupt as well as output the data onto the data bus. If a write command is in process then the WR signal performs the reset to the interrupt signal.

The bytes of data which are sent to the UPD765 to form the command phase, and are read out of the UPD765 in the result phase, must occur in a prescribed order. That is, the command code must be sent first and the other bytes sent in the prescribed sequence.

After the last byte of data in the command phase is sent to the UPD765, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the UPD765 is ready for a new command. A command may be truncated (prematurely ended) by simply sending a Terminal Count signal (TC=1). This is a convenient means of ensuring that the processor may always get the UPD765's attention even if the disk system hangs up in an abnormal manner.

In seek, the read/write head within the FDD is moved from cylinder-to-cylinder under control of the seek command. The FDC compares the present cylinder number which is the current head position with a new cylinder number, and if there is a difference the head will step in accordance with directional pulses (step in or out from spindle).

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (not ready) flag is set in status register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of the status register are set to 0 and 1 respectively.

See Appendix C for the functional details of the UPD765 Disk Controller chip.

4.5.3 Floppy Functional System Operation

Addresses 0A, 0B, and 0C hex (see Appendix G) from the Z80A-CPU control and select the disk for operation. With BA3 high, the L50 decoder is inhibited and the disk select/control decoder L30 is enabled (see Figure 4-3). With BIORQ active, one of the three outputs of the L30 decoder is selected in accordance with the addresses BA0 through BA2 from the Z80A.

NOTE

The data bus from the Z80A-CPU can initiate a disk interrupt, reset, terminal count and motor on via D4=0, D5=0, D6=0 and D7=0 respectively when floppy is actuated.

Before the floppy-disk controller (FDC) (UPD765) can read from or write to the floppy, the disk-drive motor(s) must be turned on, by MON0 and/or MON1 (see Figure 4-13). This is accomplished by the Z80A-CPU through control signal BWR and decoded instruction signal DK CNTRL and clock coded data (DB0 through DB7) into the L58 latching data buffer chip. The Z80A-CPU can also check the status of the disk drive by turning on data bus buffer L51 via DK CNTRL and BRD signals and reading the buffer's outputs.

Once there is information in the drive and its motor is running, the drive is ready to communicate with the FDC. Because RDY is tied to a high level voltage, the FDC sees the disk drive as being ready at all times. See Figure 4-13 for reference.

There are four signals from the drive that convey information: INDEX, TRACK ZERO, WRITE PROTECT and READ DATA (RDD). INDEX pulses occur once every revolution of the disk (1 revolution equals 200ms) and is active about 4.5ms. TRACK ZERO signal indicates that the drive's R/W heads are positioned at track zero (the outermost track from the spindle). WRITE PROTECT signal indicates whether a write protected diskette is installed and if so, writing will be inhibited by the drive. READ DATA consists of MFM encoded data from the disk and is sent to data separator/phase-lock loop circuits where a data window and data stream are generated before going to the FDC chip.

The input signals to the drive from the UPD765 are as follows: (See Figure 4-13.)

The DRIVE SELECT (buffer output) signal enables a particular drive's input/output lines and loads the R/W heads. The SIDE SELECT signal indicates which R/W head is selected. It should be noted that the floppy door is locked after selection until dismounted by the operator. Operator selects dismount on main menu.

When the RW/SEEK signal is high, the FDC is in the seek mode which controls the signals through one port of the L21 chip depending upon RW/SEEK polarity. When DIRECTION SELECT is made low or high, the R/W heads will step toward the spindle or away from the spindle respectively. The STEP signal moves the R/W heads one track for each pulse. When the RW/SEEK signal is low, the signals TRACK ZERO and WRITE PROTECT are enabled to the FDC.

WRITE GATE (WR GATE) enables data (WRITE DATA) to be written on the diskette. This data is a serial stream of MFM encoded signals. Prior to sending data to the disk drive, the data stream is run through a precompensation circuit which consists of a 74LS153 (L13) and a 74LS175 (L4) chip.

The precompensation circuitry is clocked at a rate of 4MHz which precompensates the data stream 125ms. The combination of this circuitry and the FDC's outputs of PS0 and PS1 (Write precompensation status during MFM mode. Determines early, late and normal times.) provide single-level precompensation.

The FDC receives a signal called WR CLK. This signal occurs at a frequency of 500KHz with the high level high for about 250ns and the low level low for 1.75ns. Other inputs to phase-lock-loop (PLL) circuit are VCO SYNC (inhibits VCO in PLL when low and enables VCO when high) and RDD DATA. VCO SYNC is an output from the FDC which enables the RDD DATA to enter the data separator whenever the FDC is doing a read operation. The $\overline{OD}$ input to the data separator/phase-lock loop is to provide a signal for the phase-lock loop to lock onto when DATA is not being read.

When doing a read operation and the PLL loop is locked on, all RD or RDD DATA clock bits occur during one polarity of the DATA WINDOW and all READ DATA bits occur during the opposite polarity.

The data bus DB0 to DB7 into the UPD765 is bidirectional. The Z80A-CPU sends commands and reads the status of the Read Data (RDD). An 8-bit status register in the UPD765 contains the status information. This information is available to the Z80A-CPU whenever it is programmed to access it. The relationship between the status registers, and the control and address signals is as shown below:

$\overline{A0}$	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

DISK SELECT from the system decoder is NAND'd with either BRD or BWR to activate RD or WR ports of the UPD765. These actions facilitate the transfer of data from the FDC to the data bus when the control signals are low. DISK SELECT also clocks a 74LS74 FF (L11) whose RESET terminal is activated by DRQ which sends an acknowledge signal (DACK) to the 765 and a DISK DRQ to port B of the PIOA on the CPU board so the Z80A-CPU can read its status through the data bus. In our application, the Z80A-CPU will let TC (terminal count) know when the disk request is complete.

The INT signal from the 765 lets the Z80A-CPU know that it desires an interrupt. This information is routed through port B of the CPU PIOA like the DRQ signal.

4.6 CRT DISPLAY AND LOGIC

The ergonomic display unit houses a 12" screen with video input and scanning circuits PCA, and the necessary controls for adjusting the display. The screen has a capacity to display a total of 1920 characters on 24 rows with 80 characters per row. Each row consists of 11 scan lines of which 8 are used to display characters, two are used for underscore and cursor, and one scan line is used for the space between rows. Each character displayed is made up from an 7 X 8 dot matrix (see Figure 4-6).

The VTAC (video timing and control) 5037 chip on the CRT/MEM PCA provides the interface between display monitor and CPU. This chip performs the logic functions required to generate all the timing signals for the presentation and formatting of non-interlaced video data on the system CRT display unit. See Appendix B for details on the 5037 VTAC chip.

4.6.1 Screen Characteristics

As stated above the number of characters in each scan line is 80 characters. Since there are a total of 24 rows with 11 horizontal scans per row, there are 264 scans per visible field. One scan line of 80 characters capacity requires 58.5us which includes the retrace time to begin the next line as well. See Figure 4-6 for screen format.

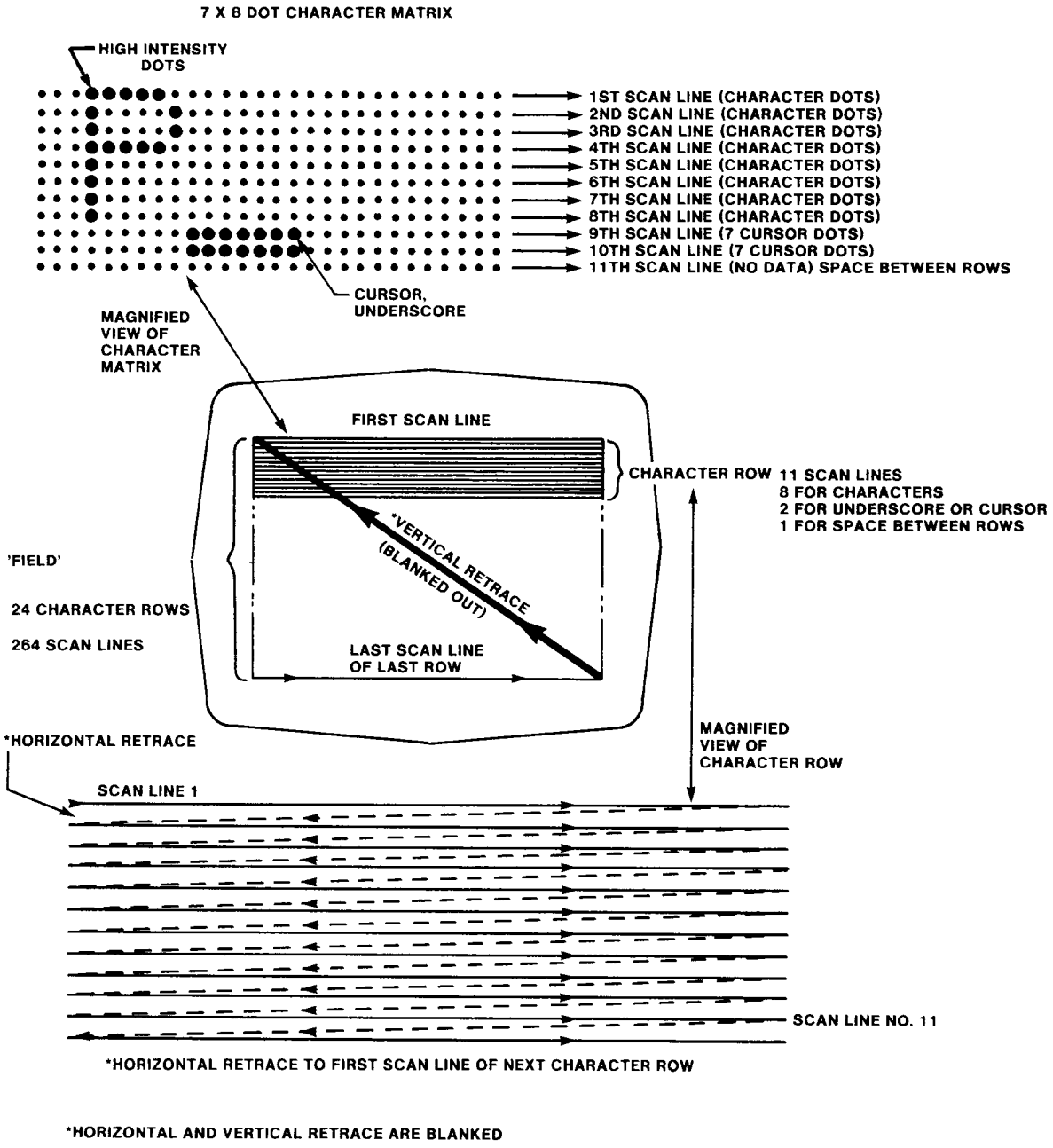


FIGURE 4-6 SCREEN FORMAT

To allow for horizontal retrace time the character count is extended to 99 counts (11 usec.). During this time a horizontal blank (BL) pulse and horizontal sync (HSYN) pulse are generated. The programmable video timing and control (VTAC) chip on the CRT/Memory board provide these and other control signals. See Appendix B for VTAC functional details.

As mentioned previously, there are 11 scan lines for each row and a total of 24 visible data rows (when screen fully loaded) which adds up to a total of 264 scan lines. An additional scan line count of 21 will occur during the vertical blank and vertical sync period. This time period permits a retrace of the scan to the the top of the screen for the start of the next display field. The total time for a vertical scan plus retrace is 16.666 ms or 60 vertical scans per second (see Figure 4-6). Data row counter outputs from the VTAC chip are DR0 through DR4. Vertical sync pulse outputs is VSYN.

4.6.2 Overview of the VTAC LSI Chip

The primary function of the VTAC is to refresh the CRT display by buffering the information from the CRT memory and keeping track of the display character positions on the screen. To this end, it provides raster timing, display row buffering, attribute decoding, cursor timing, etc.

Basically, display characters are retrieved from CRT memory and displayed on a row by row basis. The VTAC has two buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character row per frame (24) are software programmable, this information is provided by the starter/utility disk. This is also true for the number of lines per character row, the underline position, blanking of top and bottom lines, and raster timing.

Figure 4-7 shows more graphically how the characters are formed. As a line in a character row is scanned horizontally, the intensity of the CRT scanning beam is being increased and decreased in accordance with the character being formed and the position of the character on the screen. Because of the refresh rate of the lines, the tube's persistance and closeness of the dots the letters appear whole to the operator rather than being made up of individual dots as formed. The VTAC establishes the synchronous scanning times and the character generator contains the code to control the intensity of the CRT beam to form the characters. The characters to be formed are loaded into the CRT memory by the Z80A-CPU.

NOTE

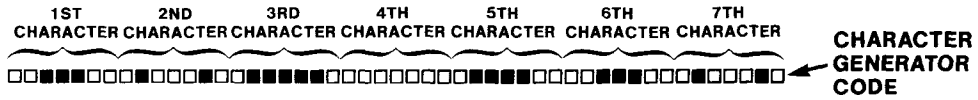
Our example in Figure 4-7 illustrates a 5 X 7 character matrix. The Wangwriter system uses a 7 X 8 character matrix.

4.6.3 CRT Functional Operation

The 4 K-byte CRT memory consists of eight 2114 chips (1024 X 4 each) which store data and associated control signals to be displayed on the monitoring unit (see Figure 4-13). Characters and attributes are written into CRT memory from system main memory by the Z80A-CPU after accessing the data from the manual keyboard or disk and storing it in the buffer section of the RAM system main memory.

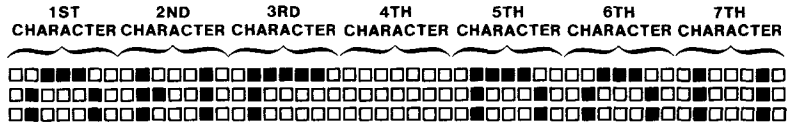
The Z80A-CPU addresses the CRT memory over a hex address range of C000 through D74F and E000 through F74F (attribute and data characters respectively). To select the CRT memory, the Z80A-CPU issues a D7=1 on the data bus during the above addresses (see Figure 4-3). With the above addresses, BA14 and BA15 to NAND gate L49 are high. During the period where BMREQ and BRFSH are low and high respectively, UMS output becomes low which enables AND gate L39-10.

Since Z80A-CPU D7=1, data bit when L50 port 03 goes high it clocks D FF L34 and latches it high. Consequently, the barred Q output becomes low and drives L39-8 low. This output signal, CRT RAM SEL, enables demultiplexer L77 (see Figure 4-13).

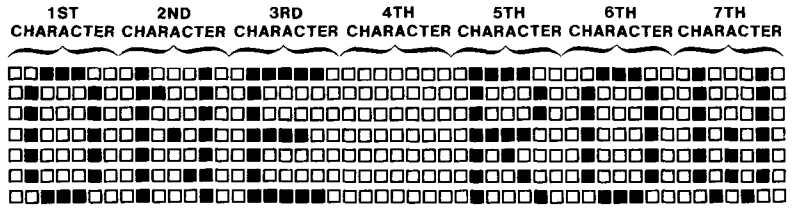


FIRST LINE OF A CHARACTER ROW

SECOND LINE OF A CHARACTER ROW



THIRD LINE OF A CHARACTER ROW



SEVENTH LINE OF A CHARACTER ROW

FIGURE 4-7 FORMATION OF CHARACTERS 5 X 7 MATRIX

When BA11, BA12 and BA13 (input to L77 demultiplexer) are low (during CRT RAM address C000 for example), 2Y0 is high, 2Y3 is high and 2Y2 is low (refer to Figure 4-13). With BWR low (active write) at the same time, the WE (Write Enable) ports of the attribute half of the CRT memory are activated. Because BA8 is also low, the left-hand half of the attribute section of memory is enabled via L26, L9, L25 and L8 multiplexer circuits. Thus the attribute memory outputs are applied to the B ports of L58 bidirectional buffer.

With BWR low and BRD high, AC buffer (L58) is enabled (port G is low) and the CC buffer (L59) is put in its high impedance state (G port is high). The BRD high signal allows the data on the data bus to pass through the AC buffer from (A-to-B ports). A0 through A9 from the Z80A-CPU selects a location in the two activated AC chips for the data to be written.

For the Z80A-CPU to read this location, BRD will be low and BWR will be high. This enables the AC buffer and allows data in memory to pass through the AC buffer B-to-A ports, putting the memory stored data on the bus for the Z80A-CPU to read.

In order to write and read the character half of the CRT memory, addresses E000 through F74F need to be addressed. These addresses will change the output code of demultiplexer L77 to accomplish the task. The other signals such as BWR, BRD and CRT RAM SEL perform the same function as they did in selecting and controlling the attribute half of the memory.

It should be noted that addresses D800 through DF7F activate the SELCG output (2Y0 of L77) and isolate the CRT memory from the data bus by placing a high level on G terminal of L58 and L59, the AC and CC directional data buffers respectively. Depending upon other conditions, which will be discussed later, SELCG will select the PROM hard-character generator L42 or the soft programmable character generator L44 and L43 RAMs.

During the periods when Z80A-CPU is not writing into or reading from the CRT memory, the VTAC chip can be addressing the memory by providing DR0 through DR4 and C0 through C6 to the multiplexers L26, L9, L25 and L8. This occurs when CRT RAM SEL becomes high placing a low on word select port of the multiplexers L26, L9 and L25. The Z80A-CPU stored character and attribute control signals are then simultaneously read from the CC and AC busses of the CRT memory.

NOTE

It should be noted when CRT RAM SEL goes high, all the demultiplexer L77 outputs (all) are forced high as well. This action isolates the CRT memory from the data bus and sets-up the 2114 chips for reading by placing a high level on WE of all memory chips.

To present data on the display, the stored CRT memory data (addressed by the character and row counters in the VTAC) must be presented to a character generator (either the PROM or soft programmable character generators) through CC0-CC7 latched buffer L41 so that the selected character generator can be addressed. The character generator in use is selected by SEL CG and CC7 control signals.

The selected character generator, is addressed by CC0-CC6 and E1, E2 and E3 (the sum of R0-R3 row select signals and derivatives of attribute signals). The output of either character generator is a dot-matrix coded signal representing a given line of the character to be displayed.

The parallel 8-bit coded signal from the selected character generator is applied to the input of an 8-bit shift register where the serial dot matrix data is extracted and applied to SSI video circuits.

The small scale integration circuits take this serial video character data and synchronizes it with CRT scanning signals developed in the VTAC. Also synchronized with the scanning signals are the attribute signals or control bits used for developing intensity, reverse video, underscore, etc. at the same time. These graphic and control signals enter L40 buffer from CRT memory at the same time the characters enter L41. They are part of the composite video presented to the CRT standard circuits.

Cursor video (CRV output of VTAC) is combined with the scanning sync pulses derived from the VTAC chip. These synchronized video and control signals are presented to the display unit via a common coaxial cable from the CRT/MEM PCB.

4.7 CRT SOFT PROGRAMMABLE CHARACTER GENERATOR

As noted earlier, in the Wangwriter system there are two character generators, a PROM and two RAM 2114 chips. The PROM of course is pre-programmed prior to being physically loaded in the system and provides a fixed character set. The RAM can be written into by the Z80A-CPU which can change the character set as desired. However, the RAM information is lost with system shut-down for example (the PROM is not volatile). Various character sets could be put on a floppy starter/utility disk and loaded into the soft programmable RAM memory at the start of the day.

4.8 VTAC PROGRAMMING

One of the major chores of the Z80A-CPU is to load VTAC during the system initialization routine. (Z80A-CPU gets the information from the starter/- utility disk.) The VTAC is program loaded as follows: (See Appendix B for additional details.)

HEX Address	PROGRAM
40	Load horizontal load count
41	Load sync width, delay, interface
42	Load scan/data row, char/data row
43	Load skew bits, data rows/frame
44	Load scan lines/frame
45	Load vertical data start
46	Load last displayed data row

Other input/output addresses are as follows:

HEX Address	PROGRAM	I/O
48	Read Cursor row address	I
49	Read Cursor character address	I/O
4A	VTAC reset	I/O
4B	Up scroll	0
4C	Load cursor character address	0
4D	Load cursor row address	0
4E	Start timing chain	I/O

4.9 PRINTING COMMUNICATIONS

4.9.1 Data Input/Output

The printer has five major circuits: daisy, carriage, paper, ribbon and hammer. Four of the circuits are functionally alike, the hammer circuit differs only a little. It uses a hammer coil to activate the hammer, and the other four circuits employ a stepping motor to drive the mechanics of the printer. Each stepper motor is controlled by four phase signals and hold line. CTC channels 0, 1 and 3 are used in the timer mode for timing the stepper motor phase changes.

The daisy stepping motor position the petals of the daisy for printing, and the carriage stepping motor phase changes position the carriage (which carries the daisy) in the horizontal plane. A paper stepping motor positions the paper in the vertical direction (line feed). The printing ribbon is also driven by a stepping motor, and the hammer strikes the petal when the daisy and carriage are in the correct printing positions. The hammer is activated by an energizing coil.

All the above circuits, except the hammer circuit, are in a servo loop with the Z80A-CPU. The Z80A-CPU causes the servo circuits to move to specific positions and the Printer PIO (through output ports) advises Z80A-CPU the status of their positions as necessary via paper out, ribbon out, left-margin and right-margin sensors for example.

The communications are bidirectional and between the Z80A-CPU and the printer. The status of the printer is read by the Z80A-CPU through the PIO chip on the printer PCA, and the printer circuits are driven by the Z80A-CPU through latching type ports. (See Figure 4-3 and 4-13.)

The addresses of the A and B status ports of the printer's PIO chip are 50 and 51 hex respectively. The latching printer input ports are addressed as follows:

Panel LEDs	--	54
Ribbon motor	--	5B
Daisy drive	--	58
Carriage	--	59
Paper drive	--	5A
Hammer fire	--	5C
Diagnostic display	--	5F

When the Z80A-CPU is programmed to determine the status of the sensors and switches tied to port A of the printer PIO for example, address (50 hex) BA4, BA5 and BA6 become high respectively, low, and high on L56 decoder respectively causing a low output on printer output port 5 (refer to Figure 4-3).

The low output of L56 decoder is inputted to L14 on Figure 4-13. With BA3 and BA2 both low, 1Y0 outputs a low which selects the printer's PIO (L13). BA0 and BA1 into the PIO selects port A data to be placed on the Z80A-CPU data bus when both are low. When RD and BIORQ of the Z80A-CPU are low, the processor will read the status data: right-margin sensor, left-margin sensor, ribbon-out switch, paper-out switch, and cover-open switch.

The status of TOF, P LOAD, LF DWN, LF UP, R DOWN, R UP and SEL (port B) switches can be determined by the Z80A-CPU in a similar manner at a specified programming time. Input B7 of the PIO in the printer indicates that the 36V enable power is applied to the printer.

At a given program time, the Z80A-CPU addresses one of the six printer input ports by hex 58, 59, 5A, 5B, 5C and 5F. For example, let's assume the Z80A-CPU wants to send new positioning data to the daisy print wheel (hex 58). Zero output of the address decoder L15(A) clocks daisy latching circuit L40. This action latches the data from Z80A-CPU to the output terminals of the latching circuit, updating its information. In turn, D01 through D04 are inputted to a drive amplifier which steps the daisy print-wheel stepping motor to a new printing position. It should be noted that the Z80A-CPU gets its position information from the timing counter circuits in the CTCA on the CPU PCA which are clocked by the printer's sensors (right and left margin sensors).

A hold signal from the Z80A-CPU via the latching circuit will hold the stepping motors at a given position.

Four of the five signals from the latching circuits also feed the NAND circuits which are tied to an input to the fault amplifier. Should the data code from the Z80A-CPU indicate a fault, the amplifier will illuminate the board LED and disable the drive circuits.

4.9.2 Stepping Motors and Driving Amplifiers

The permanent magnet stepping motors contain a stator which has a number of wire-wound poles (see Figure 4-8). Each pole has a number of teeth as part of its flux distributing member, and the rotor is cylindrical and toothed.

The PM stepping motor operates by means of the interactions between rotor magnet biasing flux and the magnetomotive forces generated by applied current in the stator windings. The pattern of winding energization is fixed, therefore; there is a series of stable equilibrium points generated around the motor. The rotor will move to the nearest of these points and remain there. If the windings are then excited in sequence, the rotor will follow the changing point of equilibrium and rotate in response to the changing pattern.

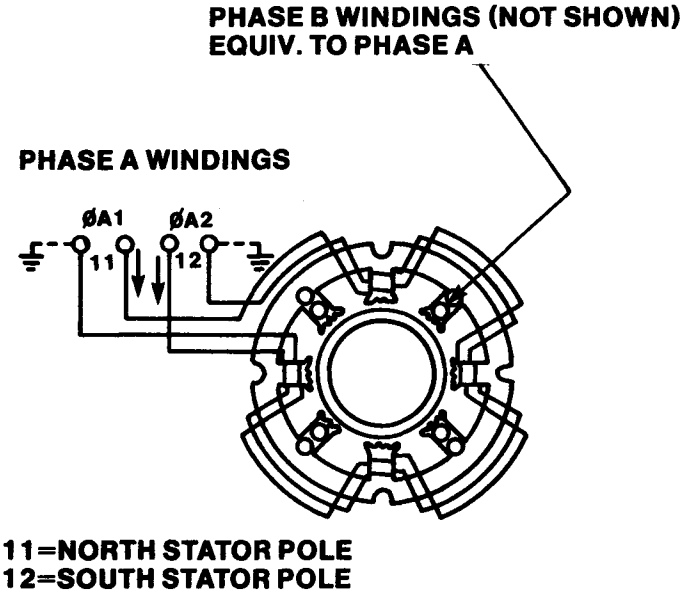


FIGURE 4-8 PERMANENT MAGNET MOTOR

A typical stepping motor drive system, accepts drive (position) signals from the CTCA via Z80A-CPU and converts them to the proper format for driving the motor windings. The power amplifier (see Figure 4-9) drives the required current through the windings, and a power return system removes the current from the windings at the termination of the step. See Figure 4-10 for drive and power waveforms.

Since the motor rotates in response to a changing pattern of interactions between the rotor magnetic field and the stator magnetic fields, the function of a state generator (not shown) is to create the proper sequence and pattern of states in response to a serial pulse train. The generator thus drives the power amplifiers that excite the stepping windings.

There are two major sequences which will cause the motor to step. One is called a "WAVE" drive in which only one set of stator poles are energized at a time. A second sequence (two-phase drive) energizes both pole sets simultaneously. Either of these will cause the step motor to step by increments of N^{o}, but there is an $N^{o}/2$ step or 1/2 step when the two sequences are alternately used. The 1/2 step is used in the Wangwriter system.

To effect high efficiency in motor driving, the chopper technique is used. Here stepping is accomplished by means of voltage modulation. With this technique, the full high voltage supply (36V) is applied to a motor winding until the correct current level is reached (see Figure 4-11). The voltage is then switched off, and the current is allowed to circulate in the motor winding (see Figure 9). When the current decays to a predetermined level, voltage is again applied to drive the current back to the correct level (see Figure 11). This cycle is continued throughout the driving pulse time. At the termination of the driving pulse, the motor winding current is recirculated or discharged rapidly to the high voltage.

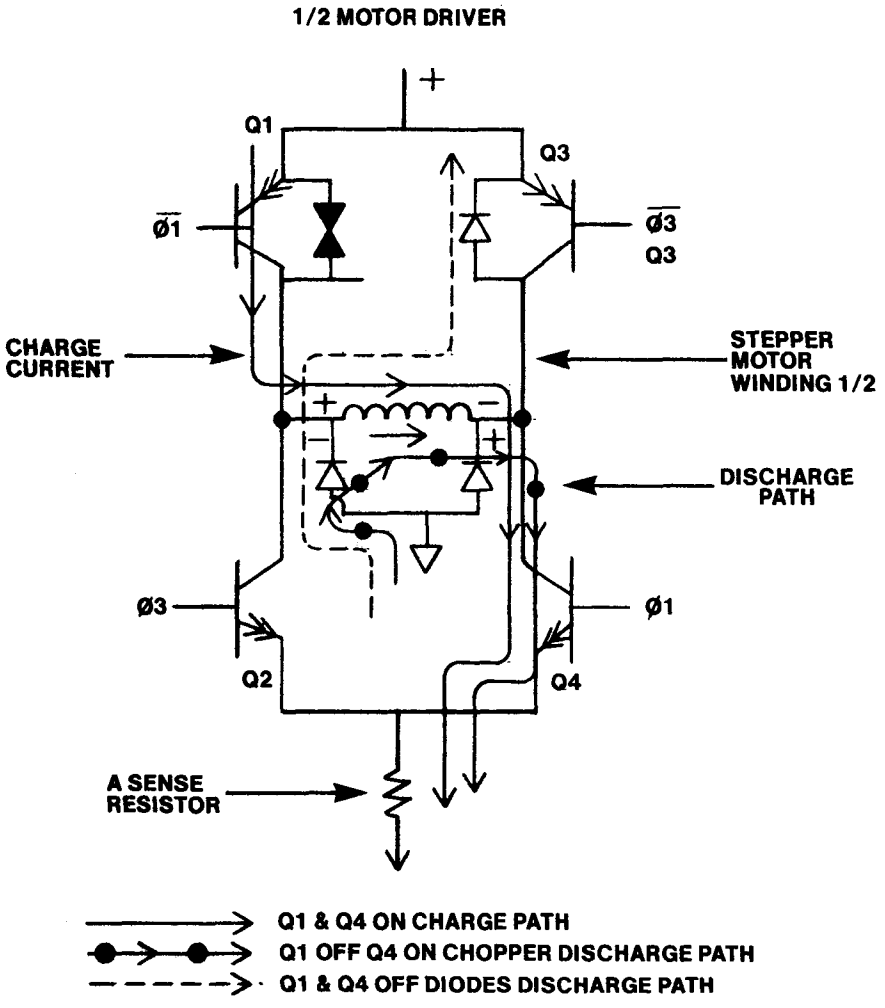


FIGURE 4-9 MOTOR DRIVER

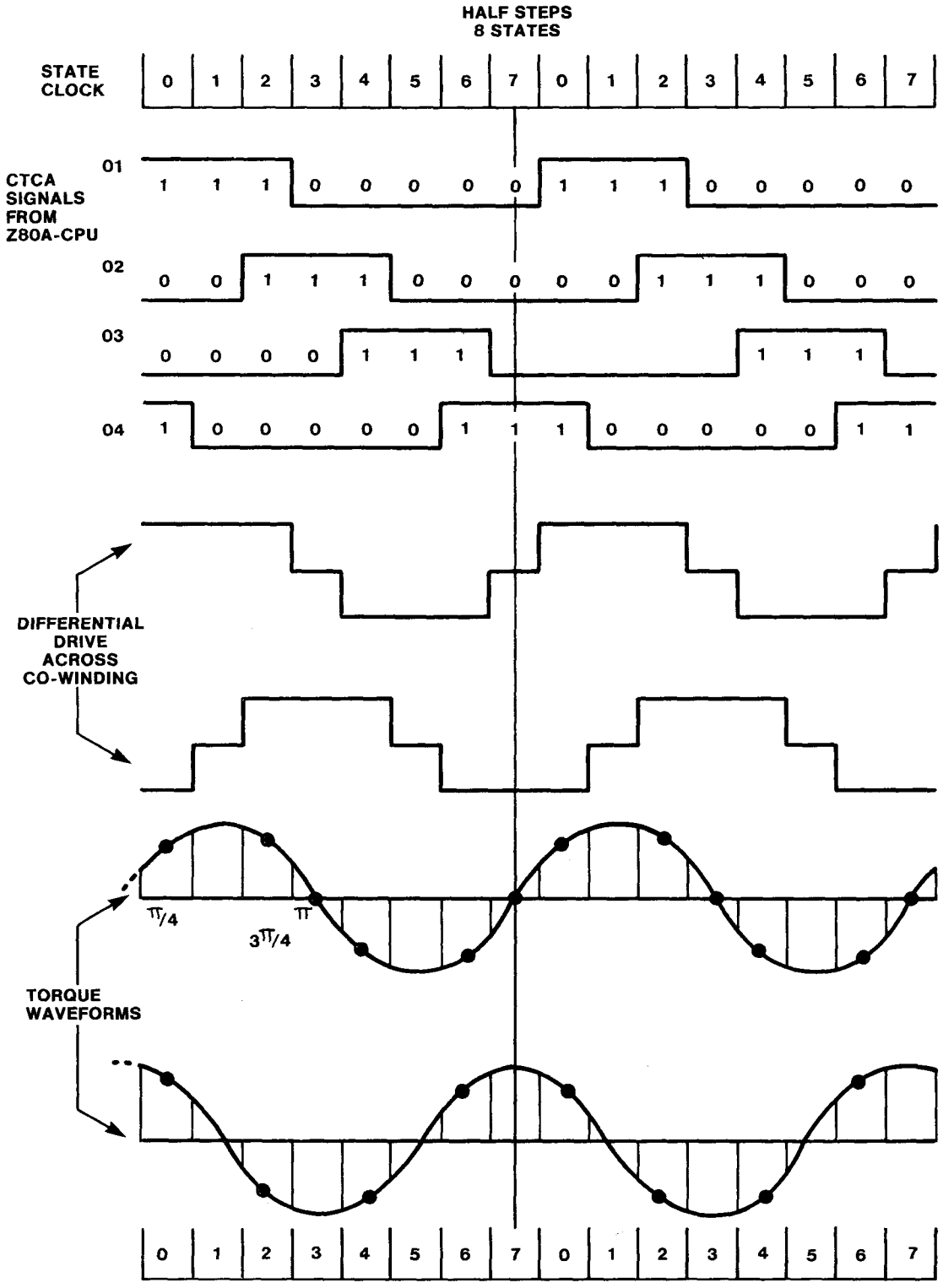


FIGURE 4-10 DRIVE AND POWER WAVEFORMS

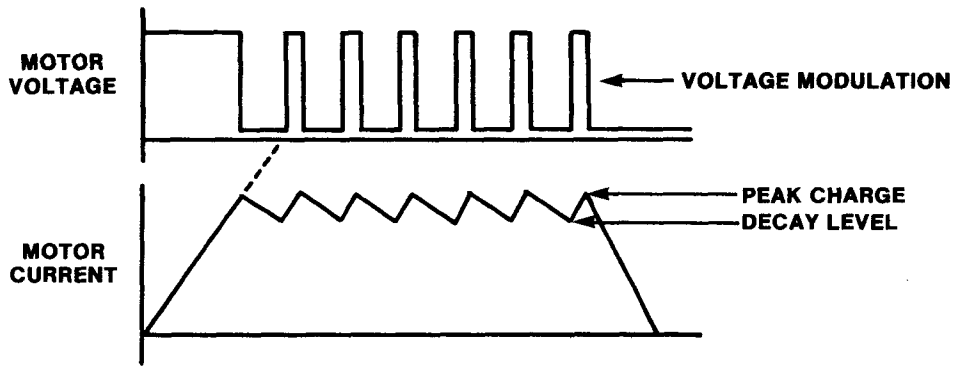


FIGURE 4-11 CHOPPER TECHNIQUE

The chopper technique is inherently well suited to start-stop applications such as the printer's carriage, printwheel, paper and ribbon circuits. The modulated high voltage is made available to accelerate the rotor as rapidly as possible, with a maximum of low frequency torque.

4.10 KEYBOARD COMMUNICATIONS

The keyboard and display units are of a mini ergonomic design. The keyboard can be placed where an operator desires because it is a separate unit and movable over a reasonable range.

Keyboard output data is serial in nature and is converted to parallel data in the CPU's UART as shown in the functional block diagram, Figure 4-13. The resultant parallel data (K0 through K6 and shift) is routed to the PIOA chip port A. The Z80A-CPU acquires this information via the data bus and then routes it to the system RAM buffer memory. From here, the Z80A-CPU will route it to the necessary peripheral devices such as the CRT memory and floppy after being stored in main memory.

The keyboard unit consists of four major components: capacitive key- board, an encoder, multiplexer, and an UART. The unit provides keyboard character and control signals to the system CPU in a serial format, and the CPU provides serial data such as alarm, clock, keyboard test and HSYNC to the
keyboard unit. Refer to keyboard schematic during the following discussions.

The AY-3-4592 encoder is a dual-pulse scanning encoder and controller for the capacitive keyboard. It contains a 4-k ROM for programming, a 128-bit shift register and an internal oscillator.

Scanning of the keyboard matrix is performed by the encoder in conjunction with an RCA 4051B multiplexer. The encoder provides a 3-bit address (YA, YB, and YC) used to scan each of the eight sense lines (Y lines). The drive lines (X lines) are each pulsed low by the encoder.

If a key is activated, the pulse is coupled from the drive to the sense lines, amplified and sent to the encode. A detection circuit is used between the output of the multiplexer and the MATIN input to the encoder. In this manner, each matrix cross-point is interrogated in turn. An internal oscillator controls the matrix scanning rate.

Each matrix intersection is given a different binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes.The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure.

When a key is depressed, matrix address from an X driver and Y input line representing that key is loaded into a 7-bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10-bit word at that address is loaded into a data holding register. This data remains valid until the next key is depressed. Two negative pulses must be detected during the MARTIN timing window for the key depression to be recognized.

The encoder feeds the data to the UART (IM6402), D1 through D7 to TBR1 through TBR7 respectively. It will convert the parallel input data to serial output data at TRO. See Appendix D for UART details. KS is developed to strobe for keyboard testing.

4.11 CTCA COMMUNICATIONS

The Z80A-Counter Timer Circuit (CTCA) is a programmable chip with four independent channels that provide counting and timing functions for Z80A-CPU microprocessor. The CTCA can also generate an interrupt vector for each separate channel (for automatic vectoring to an interrupt service routine). See Wang's reprint of ZILOG's Z80-CTC in manual I.B.1.S.0 dtd January 1980.

In the system, channel two of the CTCA is used as a general system real- time clock. In the counter mode, the channel counts vertical syncs (each count = 16.7ms) from the CRT timing (60Hz) circuitry. (The VTAC in the CRT circuitry must be initialized before the vertical sync period can be considered accurate.)

Channel 0, 1, and 3 of the CTCA are used in timer mode for timing printer stepper motors phase changes.

4.12 INTERRUPT SYSTEM

The purpose of an interrupt is to allow peripheral devices to suspend Z80A-CPU operations in an orderly manner and force the Z80A-CPU to start a given perpheral service routine. This service routine is involved with the exchange of data or status and control information between the Z80A-CPU and the peripheral. Once the service routine is completed, the Z80A-CPU returns to the operation from which it was interrupted.

The Z80A-CPU has two interrupt inputs, a software maskable interrupt and a non-maskable interrupt. The non-maskable interrupt (NMI) is not used in this System; however, the maskable interrupt is used in a daisy-chain configuration.

There are three chips tied into an interrupt daisy chain configuration. These are: CTCA, PIOA, and PIO (printer). The order of interrupt priority is in the order presented above. (See Figure 4-12 System Interrupt.)

The purpose of a generated interrupt by one of the three chips in the daisy chain is to force the Z80A-CPU to execute an interrupt service routine. For instance, their immediate service will prevent disk over-writing, and provide timely print head/horizontal stepping motor movement.

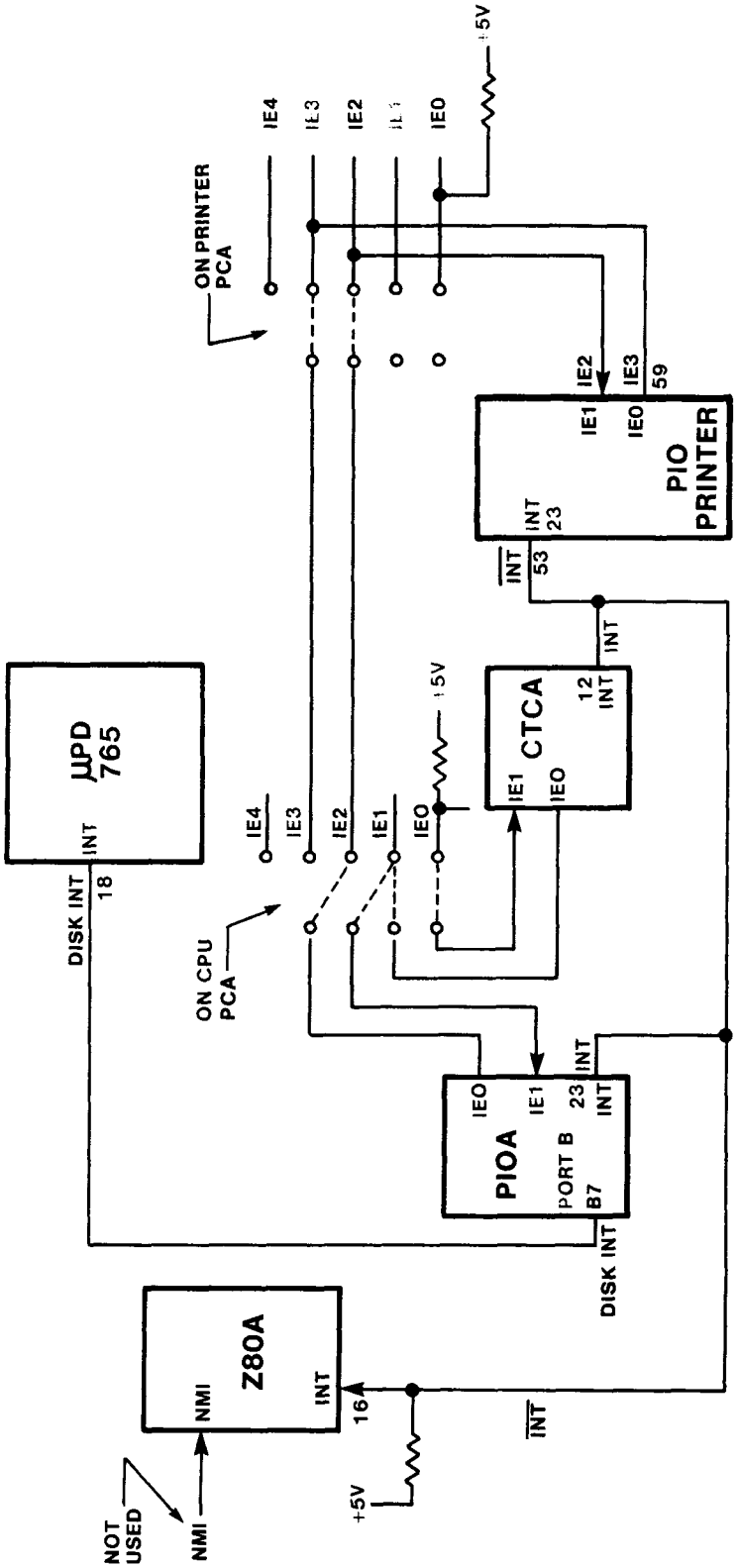


FIGURE 4-12 SYSTEM INTERRUPT

According to the Z80A-CPU interrupt protocol, lower priority devices such as PIOA and PIO (printer) may not interrupt the higher priority CTCA. However, the high priority CTCA may interrupt the servicing of the lower priority devices.

Assuming the CTCA has requested an interrupt, some time after the interrupt request, the CTCA's interrupt control logic will determine the highest priority internal channel which is requesting an interrupt. Then, in the 5503 system, the CTCA's IEI input is active, indicating that it has priority within the daisy chain, it will place an 8-bit interrupt vector on the system data bus. The high-order 5 bits of this vector will have been written to the CTCA earlier as part of the CTC initial programming process; the next two bits will be provided by the CTCA's interrupt control logic as a binary code corresponding to the highest-priority channel requesting an interrupt; finally the lower-order bit of the vector will always be zero according to a convention described below:

INTERRUPT VECTOR

D7	D6	D5	D4	D3	D2	D1	D0	
V7	V7	V5	V4	V3	X	X	0	
					0	0		Channel 0
					0	1		Channel 1
					1	0		Channel 2
					1	1		Channel 3

This interrupt vector is used to form a pointer to a location in memory where the address of the interrupt service routine is stored in a table. The vector represents the least significant 8-bits, while the CPU reads the contents of the I register to provide the most significant 8-bits of the 16-bit pointer.

Z80A 16-BIT POINTER (INTERRUPT STARTING ADDRESS)

I REGISTER CONTENTS	7 BITS FROM PERIPHERAL	0
	VECTOR	

There is a Z80A-CPU system convention that all addresses in the interrupt service routine table should have their low-order byte in an even location in memory, and their high-order byte in the next highest location in memory, which will always be odd so that the least significant bit of any interrupt vector will always be even. Hence, the least significant bit of any interrupt vector will be zero.

The RETI instruction is used at the end of any interrupt service routine to initialize the daisy chain enable line IEO for proper control of priority interrupt handling. The CTCA monitor the system data bus and decodes this instruction when it occurs. Thus the CTCA channel control logic will know when the CPU has completed servicing an interrupt, without any further communication with the CPU being necessary.

The CPU PIOA has the position of being second in priority. Within a PIOA, Port A interrupts have higher priority than those on Port B. In the byte input, byte output or bidirectional modes, an interrupt can be generated whenever a new byte transfer is requested by a peripheral. In the bit control mode, an interrupt is generated when the peripheral status matches a programmed value.

In the PIOA chip ports A and B have independent interrupt vectors. Vectoring is accomplished similar to the vectoring performed by the CTCA.

The printer's PIO is last in the priority daisy chain. It functions the same as the PIOA in the CPU. Details of operation of the PIO can be found in Wang's reprint called ZILOG Technical Manual (13-6225).

CHAPTER 5
CHECKS AND ADJUSTMENTS

Prior to the removal and replacement of suspected mechanical components, the mechanical assembly in question should be checked for proper adjustment. Should adjustment check show out-of-tolerance operation, the corresponding adjustment procedure should be performed. Should adjustment fail to correct the problem, part removal and replacement may be necessary. Adjustment and/or alignment procedures should be performed after the replacement of a given mechanical part or assembly.

For some of the subsequent adjustment procedures, the side covers of the printer must be removed to gain access to the inside of the printer. The covers are removed in accordance with the performance removal procedures in Chapter 7.

5.1 PRINTER ASSEMBLY

5.1.1 Print Wheel to Platen Check

The purpose of this check is to determine whether or not the characters on the printer Daisy wheel are positioned at the proper distance from the printer's platen. This check is made by replacing the Daisy wheel with an alignment disk and using an alignment tool to gauge the print wheel to platen gap. Proper alignment is verified if 1) it is possible to insert the alignment tool between the two with little effort and 2) there is a very slight drag on the alignment tool when it is worked back and forth between the two.

Perform the print wheel to platen adjustment (para 5.1.2) once this check has been made only if the check shows to be incorrect.

Perform the following steps to check the print wheel to platen gap:

1. With system power off, remove the print wheel from the carriage motor assembly. (Refer to Print Wheel Replacement Procedure - Chapter 7)

NOTE

Be certain to support assembly by grasping Hammar Housing assembly with one hand while performing step 2.

2. Insert alignment disk (WL #580-0152) in place of the Print Wheel (alignment disk's raised side should be positioned toward the hub). (See Figure 5-1.) Alignment disk is held in place by a knob (WL #655-0274).

3. Lift bail roller assembly away from platen.

4. Return daisy motor assembly to its normal operating position (holding by hammer housing assembly). Be certain the carriage motor assembly is properly seated.

5. Set the small end of the alignment tool (WL #726-9727) forward on the platen in line with the alignment disk (Fig. 5-2).

6. With the alignment disk and alignment tool in position and the copy control lever in position 1 indent, it should be possible to remove/insert alignment tool with only a slight drag.

NOTE

Under these circumstances, the gap between the platen and print wheel will be within 0.090 and 0.095 inch (0228 and 0.241 cm). (See Figure 5-3.)

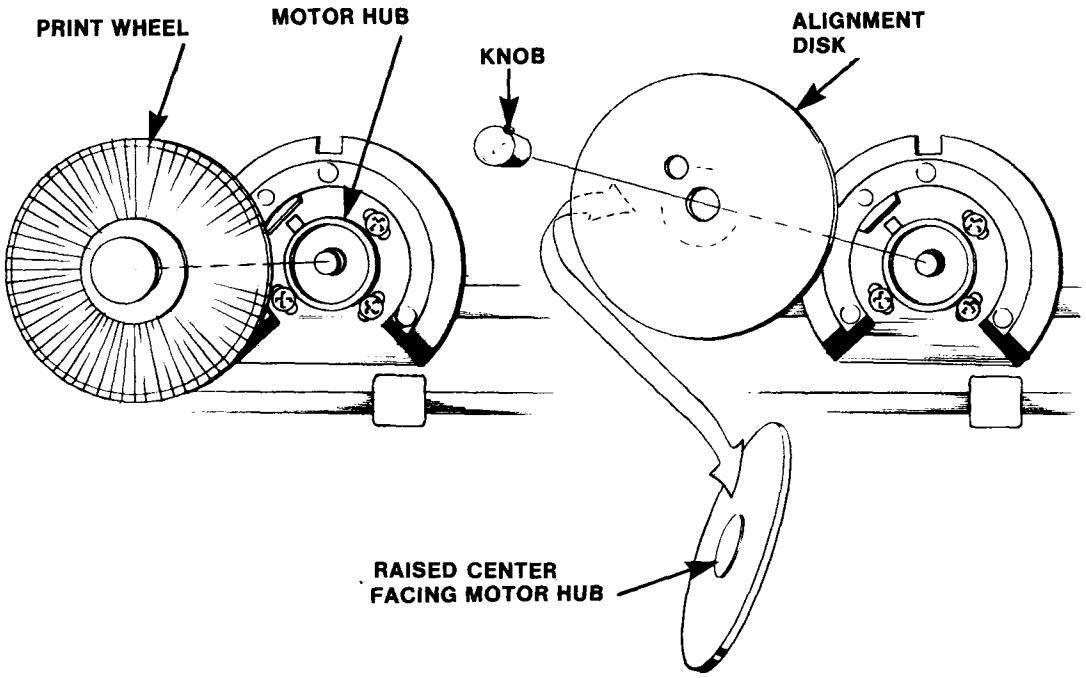


FIGURE 5-1 PRINT WHEEL AND ALIGNMENT DISKS

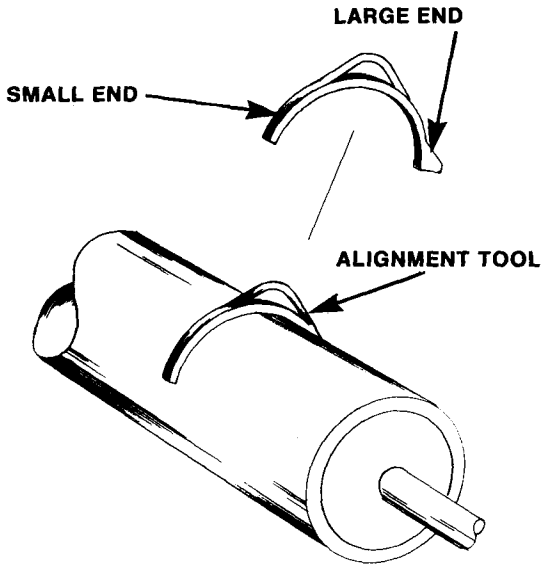


FIGURE 5-2
ALIGNMENT TOOL USING SMALL END

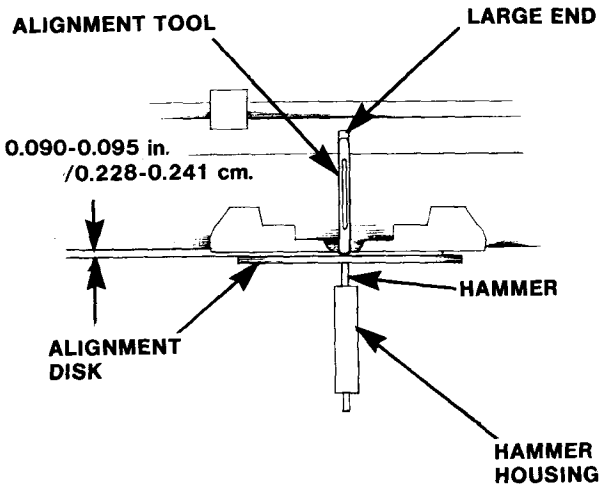


FIGURE 5-3
PRINT WHEEL-TO-PLATEN SPACING

7. Rotate print wheel approximately 180 degrees and ensure a happy medium at both positions.

8. Remove alignment tool, knob, and alignment disk (by grasping the alignment disk perimeter.

9. Replace print wheel. Put carriage assembly in its normal operating position. Replace ribbon.

5.1.2 Print Wheel to Platen Adjustment

1. With system power off, remove the print wheel from the carriage assembly. (Refer to Print Wheel Replacement Procedure - Chapter 7)

2. Remove Print Wheel by grasping and pulling hub firmly to release.

NOTE

Be certain to support assembly by grasping Hammer Housing assembly with one hand while performing step 3.

3. Insert alignment disk (WL #580-0152) in place of the Print Wheel (alignment disk's raised side should be positioned toward the hub). (See Figure 5-1.) Alignment disk is held in place by a knob (WL #655-0274).

4. Lift bail roller assembly away from platen.

5. Return carriage assembly to its normal operating position (holding by hammer housing assembly). Be certain the daisy assembly is properly seated.

6. Set the small end of the alignment tool (WL #726-9727) forward on the platen in line with the alignment disk (Fig. 5-2).

7. Loosen four phillips head screws on the carriage assembly (Fig. 5-4) and then tighten them so they are only slightly snug.

8. Snap the daisy motor assembly into its normal operating position (grasp by hammer housing).

9. Set the small end of the alignment tool (WL #726-9727) forward on the platen in line with the alignment disk (Fig. 5-2).

10. Adjust the position of the carriage assembly (as allowed by the four loose screws) such that:
    a. The alignment tool may be inserted loosely between the alignment disk and the platen and
    b. The carriage assembly is parallel with the platen and with carriage base plate (the assembly on which it is mounted, Fig. 5-4).

11. Tighten the four phillips head screws and repeat the check as a rough adjustment.

12. Remove alignment tool and alignment disk; replace print wheel and ribbon.

13. Return printer to normal operating condition and print a test document which contains lines of all capital letters.

14. Check printout for even printing of all characters and repeat portions of this procedure as necessary to achieve normal printing.

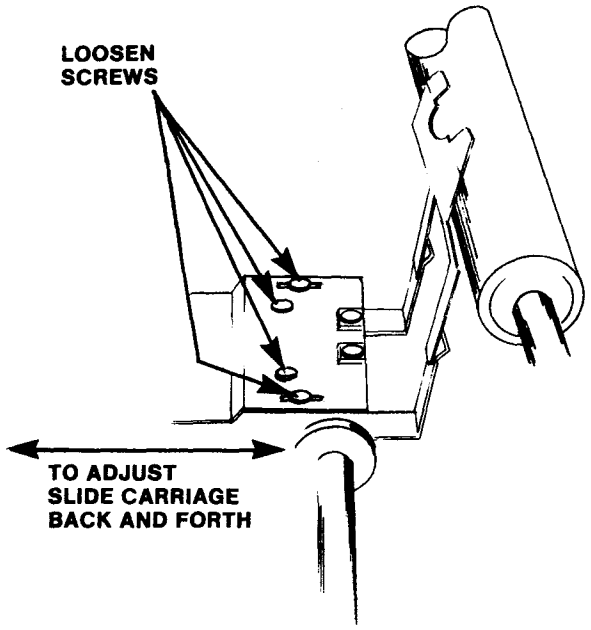


FIGURE 5-4 PRINT WHEEL TO PLATEN ADJUSTMENT

5.1.3 Hammer to Platen Check

1. Remove the print wheel.

2. Set the large part of the alignment tool (WL #726-9727) forward on the platen in line with print hammer (see Figures 5.5 and 5.6).

3. With the print wheel removed and the copy-control lever in position 1, the large end of the alignment tool should just touch the hammer.

NOTE

Under these conditions, the gap between the platen and hammer will be within 0.235 to 0.243 inch (0.597 to 0.617 cm).

4. Perform the adjustment procedure (para. 9.3) if necessary. Otherwise, return the printer to normal operating conditions.

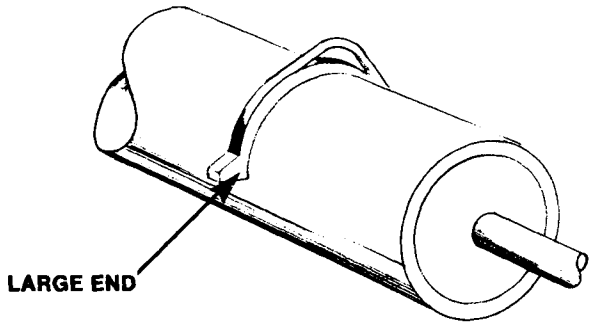
5.1.4 Hammer-To-Platen Adjustment

To adjust for the proper clearance between the hammer and the platen, perform the following procedure.

1. With the large end of the alignment tool on the platen between the platen and the hammer, loosen the two screws that mount the yoke assembly to the motor (see Figure 5.7).

2. Move the yoke assembly until the hammer just touches the large end of the alignment tool.

3. Tighten the two screws and return the printer to its normal operating condition.



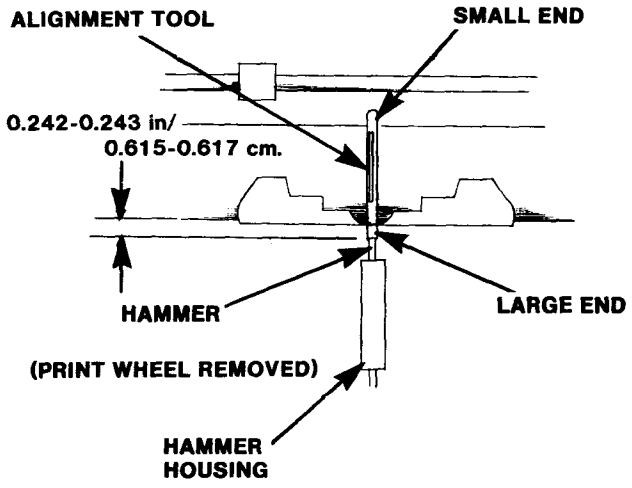


FIGURE 5-5
ALIGNMENT TOOL USING LARGE END

FIGURE 5-6
HAMMER-TO-PLATEN CHECK

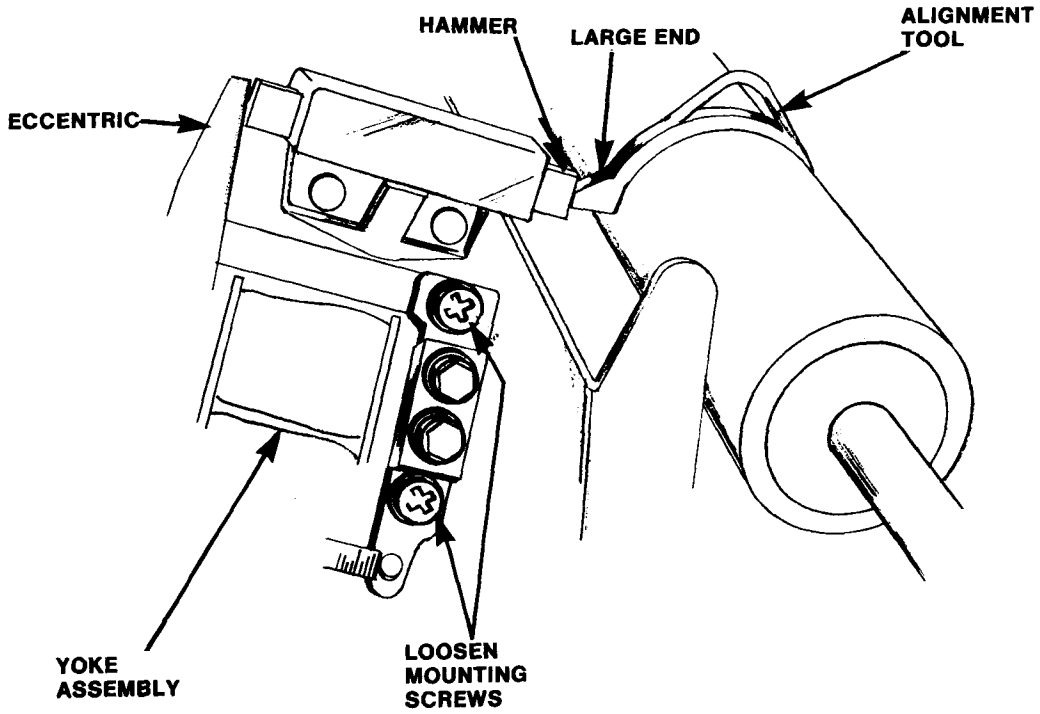


FIGURE 5-7 HAMMER-TO-PLATEN ADJUSTMENT

5.1.5 Print Hammer Angle Check

1. Print a test document with lines of capital letters (especially M's and H's).

2. Perform the print hammer angle adjustment (para. 5.1.6) if characters do not print with the same density at both the top and bottom of each character.

5.1.6 Print Hammer Angle Adjustment

1. Loosen the two hammer housing mounting/adjusting screws (Fig. 5-8).

2. Shift the angle of the hammer and hammer housing such that more even pressure will be exerted on the characters during printing and tighten the two screws.

3. Print a test document with lines of capital letters (especially M's and H's).

4. If characters do not print with the same density at both the top and bottom of each character, repeat this adjustment.

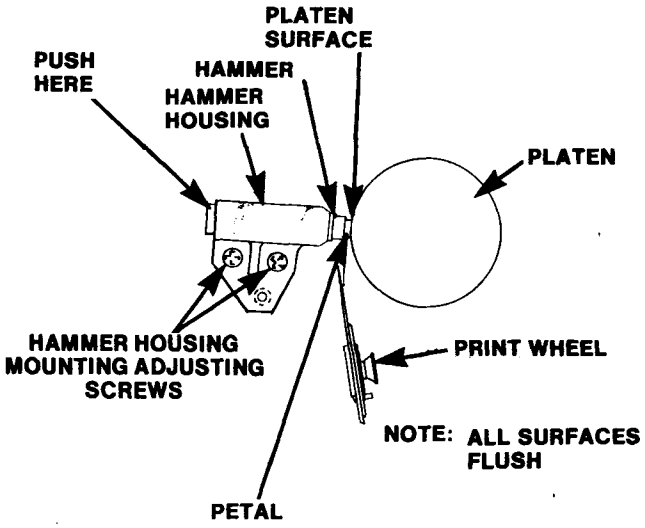


FIGURE 5-8 HAMMER CHECK AND ADJUSTMENT

5.1.7 Print Wheel Home Position Check

1. Turn power ON
2. Load operating system software and observe menu on screen.
3. Remove ribbon.
4. Select printer.
5. Pull carriage assembly back.
6. Check to see if the print wheel home position (lower case letter o) is in its normal position in line with the hammer as shown in Figure 5-9a. If not in alignment, note how far off the lower case o is from normal position.
7. Perform the home position character adjustment below.

5.1.8 Print Wheel Home Position Adjustment

If the home character position is off by two adjust photo sensor via the following steps (adjustments of less than one should be performed at depot level; see Appendix K):

1. De-select printer.
2. Pull carriage assembly back to service position.
3. Remove print wheel.
4. Loosen 2 mounting nuts (see Figure 5-10).
5. Move sensor to right if lower case o was to the left of home position and vice versa. Tighten nuts.
6. Put print wheel on.

CAUTION

Never leave carriage in service position when selecting printer.

7. Select printer.
8. Pull carriage assembly back.
9. Observe home position alignment.

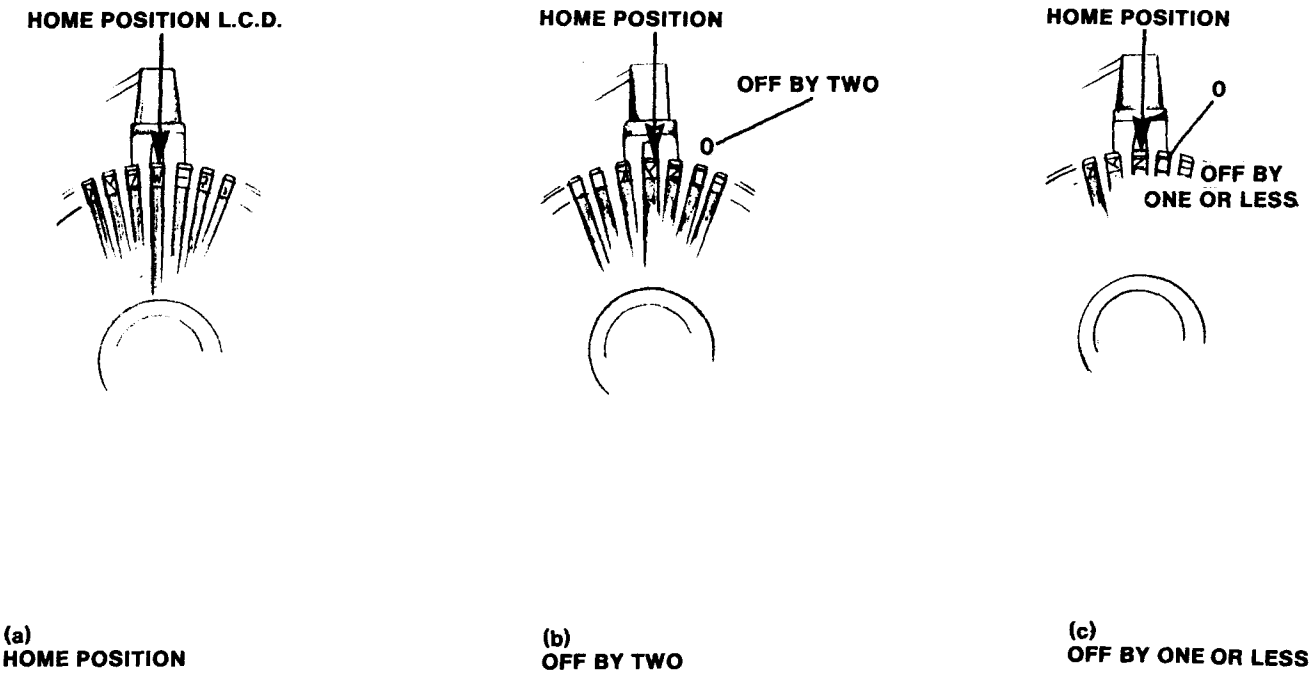


FIGURE 5-9 PRINT WHEEL POSITIONS

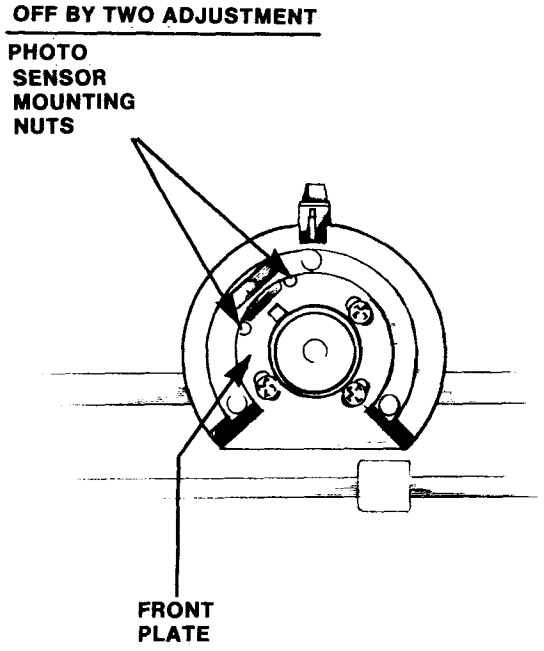


FIGURE 5-10 HOME POSITION ADJUSTMENTS

5.1.9 Print Solenoid Arm and Lamination Check

1. Remove the ribbon cartridge and print wheel (see Chapter 7 for details if necessary).
2. Push print solenoid arm all the way forward towards the platen.
3. Inspect the alignment of the print solenoid arm with respect to the face of the coil laminations and be sure that both surfaces are touching and parallel (see Figure 5-11). Should alignment be unsatisfactory, the adjustment should be performed at depot level (see Appendix K).

5.1.10 Print Solenoid Arm-to-Lamination Gap Check

Check that a 0.030 inch (0.0762 cm) gap exists between print solenoid arm and the top corner of the coil laminations as shown in Figure 5-12.

5.1.11 Print Solenoid Arm-To-Lamination Gap Adjustment

1. To adjust print solenoid arm-to-lamination gap, loosen the lock nut on the print solenoid arm stop eccentric (see Figure 5-12).

2. Adjust eccentric stop until the correct dimension is obtained (0.030 inch, 0.0762 cm).

3. Tighten lock nut.

4. Recheck hammer-to-platen check.

5.1.12 Cord Tension Check

Check the tension of the carriage cord when the carriage is on the left side. The tension should be 6 $\pm$ 1 kilograms (13.2 $\pm$ 2.2 lbs).

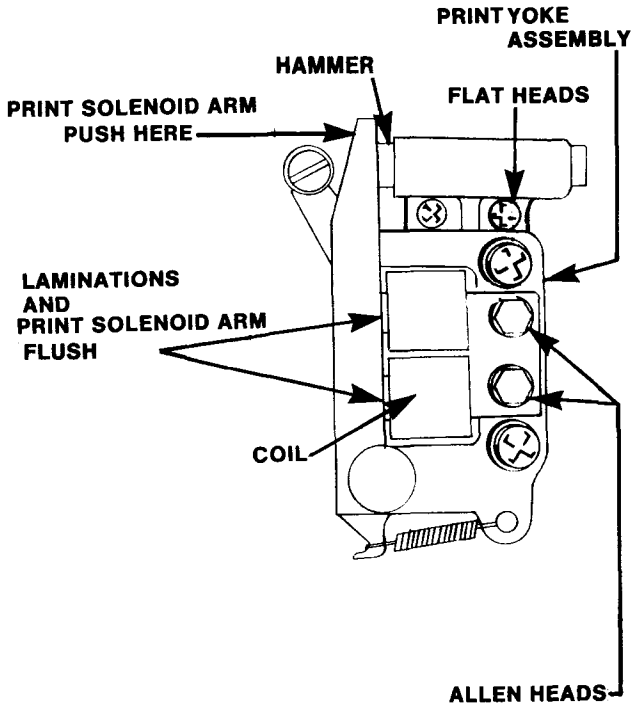


FIGURE 5-11 PRINT SOLENOID ARM AND LAMINATION ADJ.

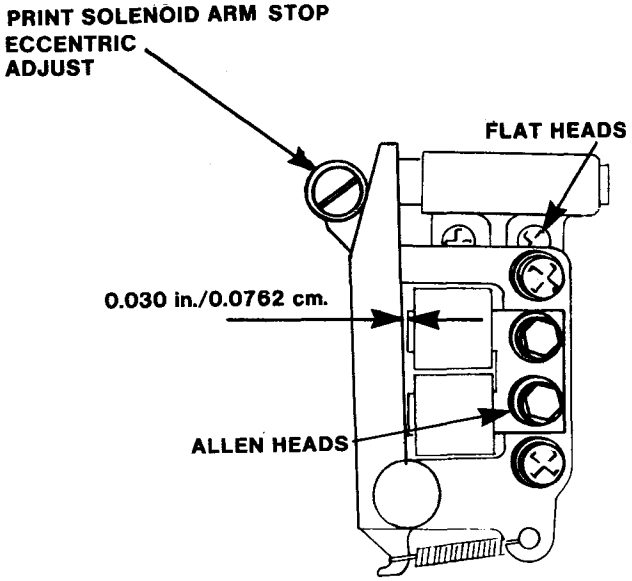


FIGURE 5-12 PRINT SOLENOID ARM TO-LAMINATION GAP

5.1.13 Cord Tension Adjustment

1. Remove right side cover.
2. Loosen lock nut (see Figure 5-13).
3. Adjust tension of cord by turning the tension screw on the right side of the printer (see Figure 5-13).
4. Adjust the screw in-or-out to achieve the correct tension when the carriage is on the left side of unit. Tighten lock nut.
5. Re-install side cover.

5.1.14 Backlash Check

1. Turn power on.
2. Load as software.
3. Select printer.
4. Check backlash by rotating platen gear back and forth.
5. Deselect and rotate platen 90°.
6. Select the printer, and check for backlash again.
7. Repeat steps 5 and 6 until full 360° revolution is checked.

NOTE

Only a small amount of movement is acceptable.
If excessive, perform adjustment below.

5.1.15 Backlash Adjustment

1. Remove disk and then power.
2. Remove printer (see Chapter 7).
3. Loosen the idler gear locking screw and adjust the eccentric screw so that the backlash between the drive gear and idler gear is minimum (see Figure 5-14).

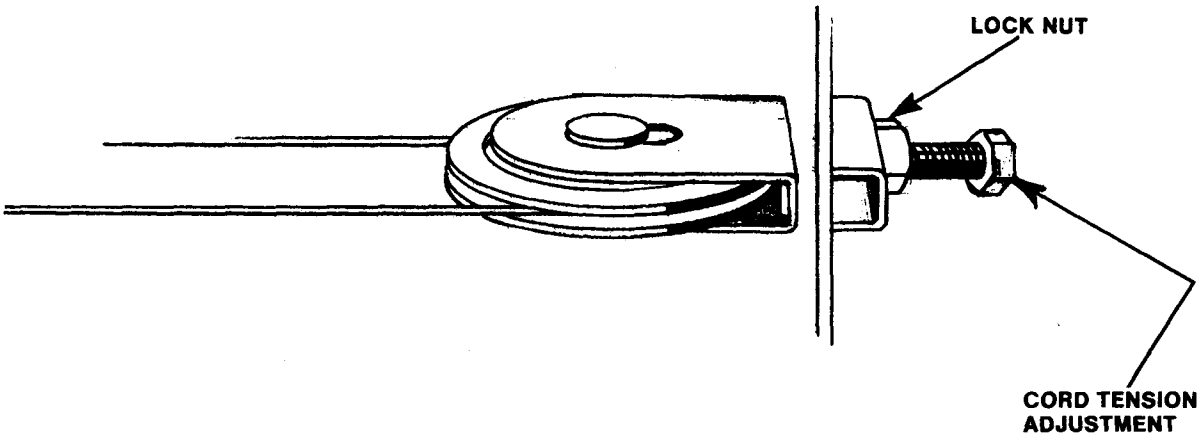


FIGURE 5-13 CORD TENSION ADJUSTMENT

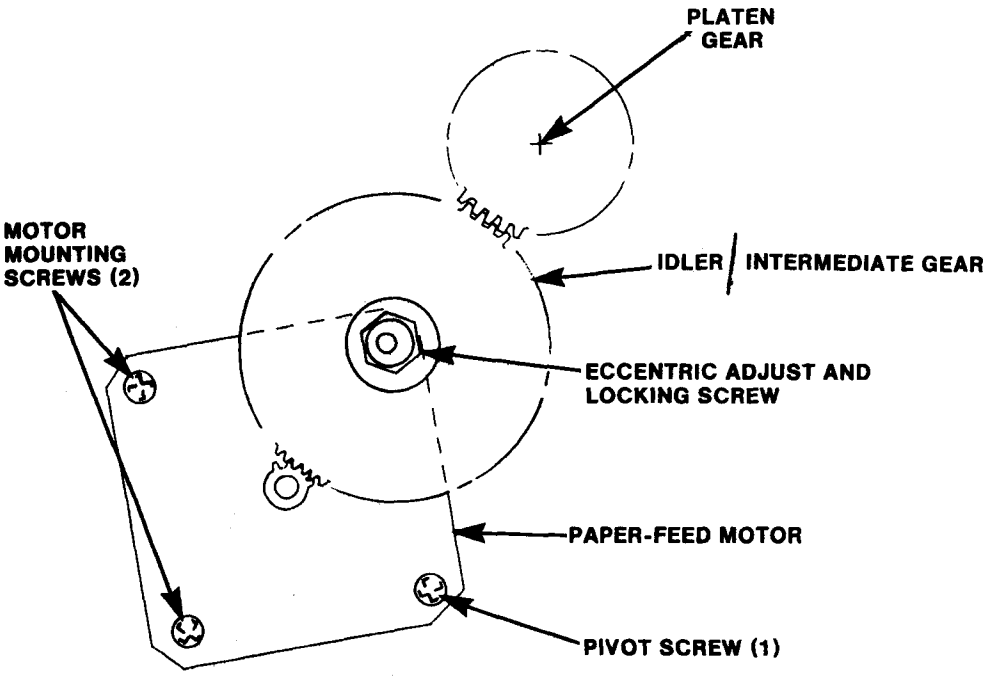


FIGURE 5-14 BACKLASH CHECK AND ALIGNMENT

NOTE

Moving gears closer together reduces backlash. However, moving gears too close together will cause binding of gear train. Check each adjustment for binding before continuing with procedures. Turn gears through 360° while checking.

4. Tighten gear nut while holding eccentric nut in place.
5. Loosen the three motor mounting screws on plate and adjust the backlash between the idler gear and platen gear (see Figure 5-14).
6. Tighten the three mounting screws while holding plate.
7. Install printer.
8) Perform the backlash check again to determine the amount of backlash after adjustment.

5.1.16 Card Guide Check

1. Turn power on.
2. Load OS (operating system) software.
3. Remove OS software diskette.
4. Load document for printing.
5. Select Print Document.
6. Name document.
7. Execute.
8. Selecting printing parameters.
9. Execute.
10. Insert paper.
11. Select Printer.
12. Print two lines, at least.
13. Check that the printing is horizontally aligned with the horizontal segment of the card guide as shown in Figure 5-15. Either the roll-up or the roll-down switch may be used to position the line of characters.

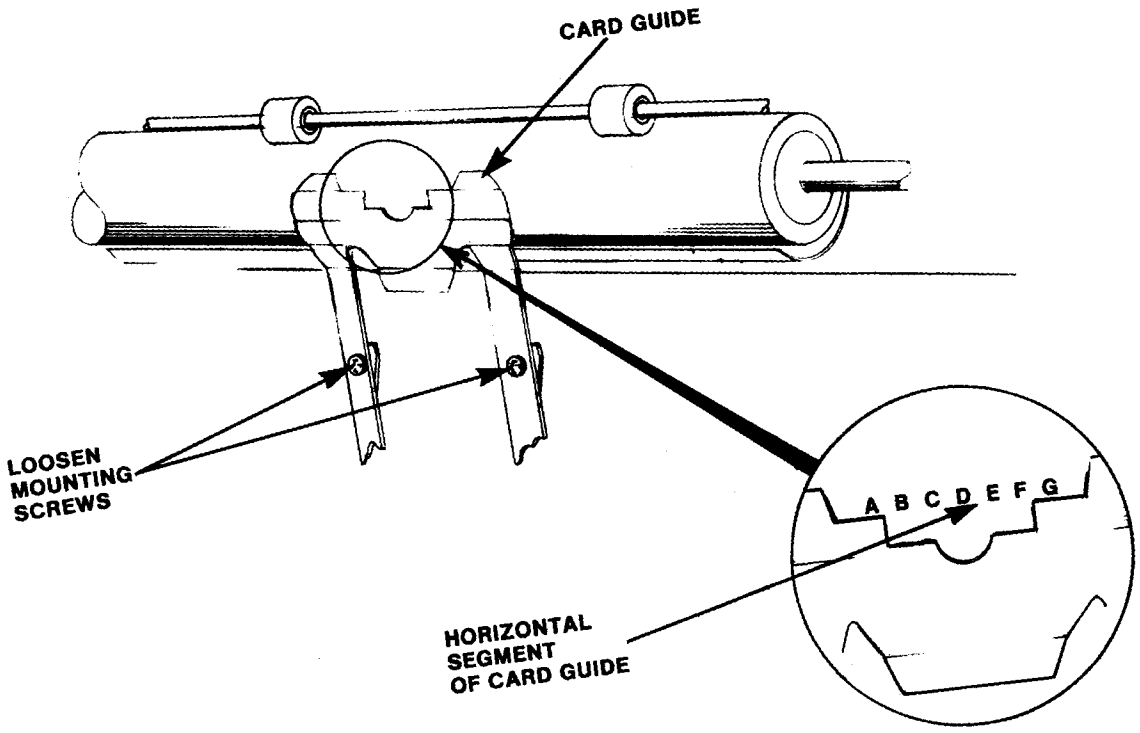


FIGURE 5-15 CARD GUIDE CHECK AND ADJUSTMENT

NOTE

If not in alignment perform the adjustment.

5.1.17 Card Guide Adjustment

1. Loosen the two card-guide mounting screws (see Figure 5-15).

2. Move card guide so that the horizontal segment of the card guide is parallel to the previously printed material.

3. Hold guide stationary and tighten screws.

5.1.18 Left Margin Home Position Check

1. Turn power on.
2. Load OS software.
3. Remove OS software diskette.
4. Load document disk.
5. Select Print Document on menu.
6. Name document.
7. Execute.
8. Select printing parameters, left margin at 00.
9. Execute.
10. Insert Paper.
11. Select printer.
12. Print several lines.
13. Check that the left-margin home position is 0.55 $\pm$ 0.016 inch (1.4 $\pm$ 0.04 cm) from the left side of the paper to be printed on when the margin is set at 00 on the print menu.

5.1.19 Left Margin Home Position Adjustment

1. Loosen the screw that holds the photo flag (see Figure 5-16).

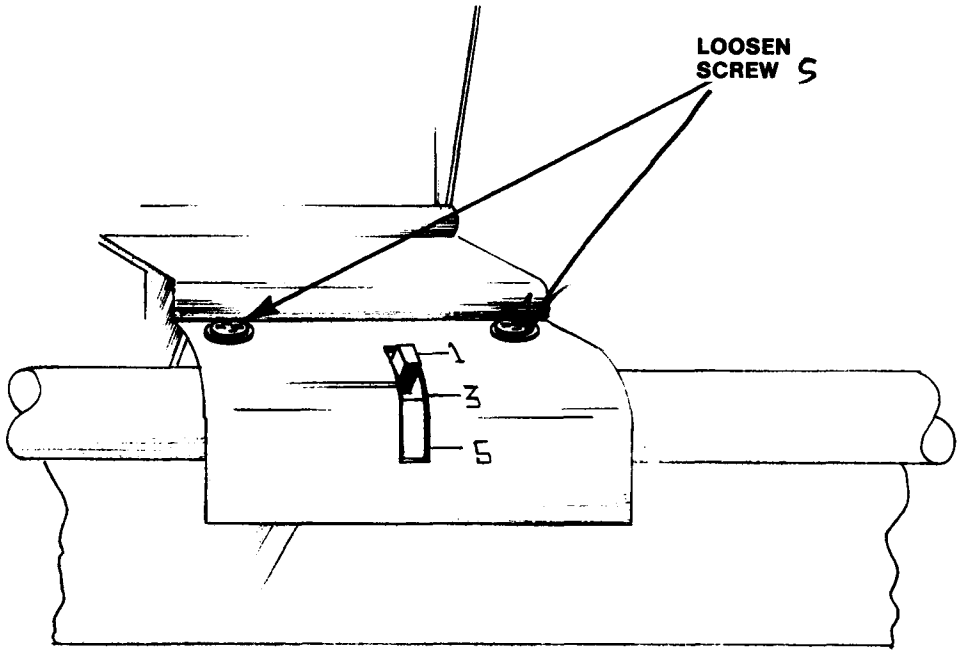


FIGURE 5-16 LEFT MARGIN HOME POSITION ADJUSTMENT

NOTE

Moving photo flag towards the left increases the left margin width. Moving photo flag towards the right decreases margin width.

2. Slide the photo flag from side-to-side until left margin is 0.55 ± 0.016 inch (1.4 cm) from left side.

NOTE

This is accomplished by re-cuing the document and re-adjusting the flag until the left margin is at 0.55 ± 0.016 inch (1.4 cm).

5.1.20 End of Ribbon Check

1. Make test ribbon cartridge:

   a) Obtain used cartridge.
   b) Cut ribbon so the metal spring in sensor pocket reflects LED light.

2. Insert test cartridge in system.

3. Turn on system and load OS software.

4. Observe LED light (change ribbon) on printer keyboard. It should be illuminated.

NOTE

If LED is not illuminated, adjust sensor.

5. An optional method of checking that the sensor is good consists of putting a flat metal tool such as feeler gauge or screwdriver tip in front of the sensor (must be able to reflect light). This activates the change ribbon light.

5.1.21 End-of-Ribbon Adjustment

1. Loosen mounting screws on sensor.

NOTE

Move carriage over hole in cross frame so screw driver can be used to loosen screws on bottom of sensor.

2. Adjust sensor so that its active side is parallel to the pocket in the ribbon it fits into under normal operation.

3. Perform the above check again to be sure change ribbon panel LED illuminates.

5.1.22 +12 and +5 Vdc Checks and Adjustments

NOTE

R1=+12Vdc and R2=+5Vdc on the regulator board in the power supply drawer. The potentiometers are located at the upper right-hand corner of the regulator board. The left is +12Vdc pot and the right is the +5Vdc pot.

1. Turn power off and remove the sides of the printer cabinet. (See Chapter 7 for details if necessary.)

2. Remove the two screws on each side of the power supply. (Refer to Chapter 7 if necessary for screw locations.)

3. Fasten the negative lead of the voltmeter to printer PCA J1 pin 61 or 62.

4. Fasten the positive lead of the voltmeter to Printer PCA J1 pin 5 or 6.

5. Turn system ON.

NOTE

If reading is within +11.40 to +12.60, adjustment is not necessary. If voltage is not within range, adjust R1 as close as possible to nominal reading of the above range (12Vdc). If adjustment is impossible, first replace the regulator PCA and heat sink subassembly and then the power supply. See Chapter 7 for removal procedure.

6. Fasten the positive lead of the voltmeter to Printer PCA J1 pin 1.

NOTE

If reading is within 4.75 to 5.25, adjustment is not necessary. If voltage is not within range, adjust R2 as close as possible to nominal reading of the above range (+5Vdc). If adjustment is impossible, first replace regulator and heat subassembly and then the power supply. See Chapter 7 for removal procedures.

5.2 FLOPPY DISK

The system contains a prom-loaded routine for performance of the floppy disk checks and adjustments. To initiate the routine:

1. Within 2 seconds of power turn-on, depress CANCEL.

2. Within 2 seconds of depressing CANCEL, depress INDENT. The prom-loaded routine should be active at this point.

CAUTION

Adjustments to the disk drive may render the drive unable to read previously written diskettes. The customer should be made aware of this possibility should adjustments or replacements be necessary.

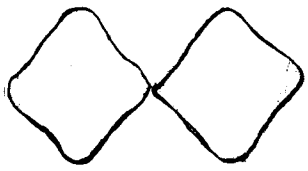
5.2.1 Radial-Track Alignment Check

1. Remove left-side and right-side covers of the stand (see Chapter 7).
2. Insert a CE alignment diskette (Wang Part No. 726-8068) and close the door.
3. Press keyboard numeric key 0 (zero) for system software to set the drive to track 00.
4. Sync scope on leading edge of index signal at TP6 on the disk drive PCA (see Figure 5-17).
5. Connect channel A probe to TP1 and channel B probe to TP2 (head signals, see Figure 5-17).

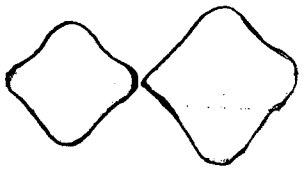
NOTE

Set scope to 50mV/cm, ac coupled, channel A and B added, with B inverted, 20 ms/div. Attach ground probes to the ground end of capacitor C30 and C31 (see Figure 5-18).

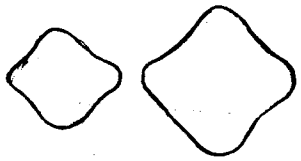
6. Press keyboard key 4.



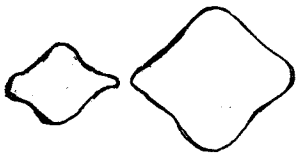
EQUAL AMPLITUDE
(ON TRACK 16)



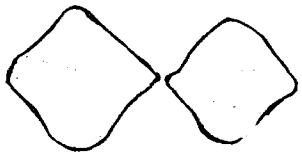
LEFT 80% OF RIGHT
(-1 MIL OFF TRACK, TOWARD 15)



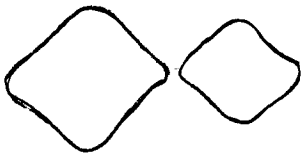
LEFT 60% OF RIGHT
(-2 MIL OFF TRACK, TOWARD 15)



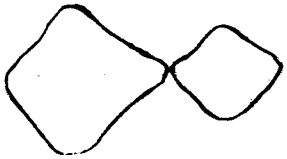
LEFT 40% OF RIGHT
(-3 MIL OFF TRACK, TOWARD 15)



RIGHT 80% OF LEFT
(+1 MIL OFF TRACK, TOWARD 17)



RIGHT 60% OF LEFT
(+2 MIL OFF TRACK, TOWARD 17)



RIGHT 40% OF LEFT
(+3 MIL OFF TRACK, TOWARD 17)

FIGURE 5-19 TRACK SIGNALS

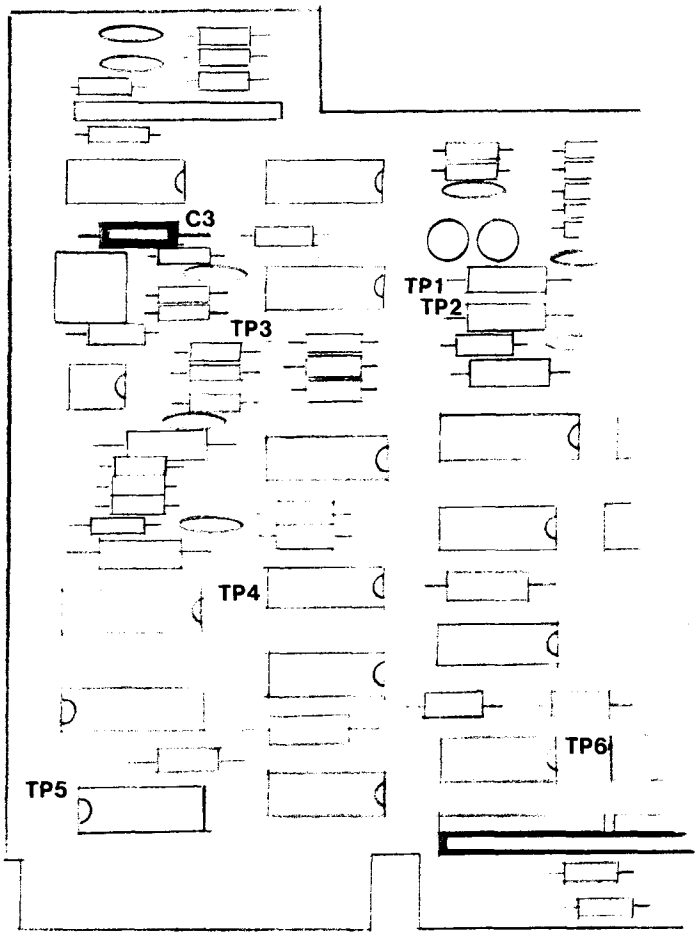


FIGURE 5-17 LEFT SIDE OF FLOPPY PCB

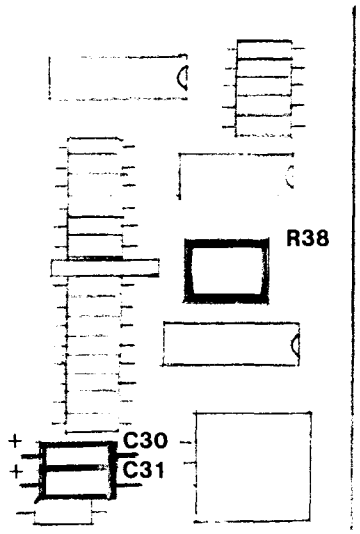


FIGURE 5-18 FLOPPY MIDDLE RIGHT OF PCB

NOTE

The carriage should now be located at track 16. The proper phase relationship of stepper motor phases should be: phase 4 and 1 (J4-23 and 26) = 0V, phase 2 and 3 (J4-25 and 24) = +12V.

7. Check that the cats-eye pattern (see Figure 5-19) appears on the scope with equal amplitude. If not, adjust as described in paragraph 5.2.2.

5.2.2 Radial-Track Alignment

1. Perform the set-up in paragraph 5.2.1.

2. With power on, loosen the set screw (see Figure 5-20) in the stepper pulley (using the 0.050 hex wrench) and position the pulley so that the pattern (see Figure 5.19) appears on the scope with equal amplitude.

3. Secure the pulley set screw with 2 inch-pound of torque.

4. To verify alignment, command a return to track 00 (hit 0 key) and then step forward to track 16 (key 4). Also command a seek to track 32 (key 5), and then step back to track 16 by hitting key 4. (Both stepping sequences should produce equal amplitude at track 16.)

5.2.3 Index-to-Data Check (Oscilloscope set as in paragraph 5.2.1)

1. Verify the radial-track alignment (refer to paragraph 5.2.2).
2. Move the head to track 01 (key 1).
3. Set the horizontal amplifier of the oscilloscope to 50 microseconds per division.
4. Check that the scope shows a data pattern starting 200 $\pm$ 50 microseconds from the start of the trace (see Figure 5-21).
5. If out of tolerance, perform procedure in paragraph 5.2.4.

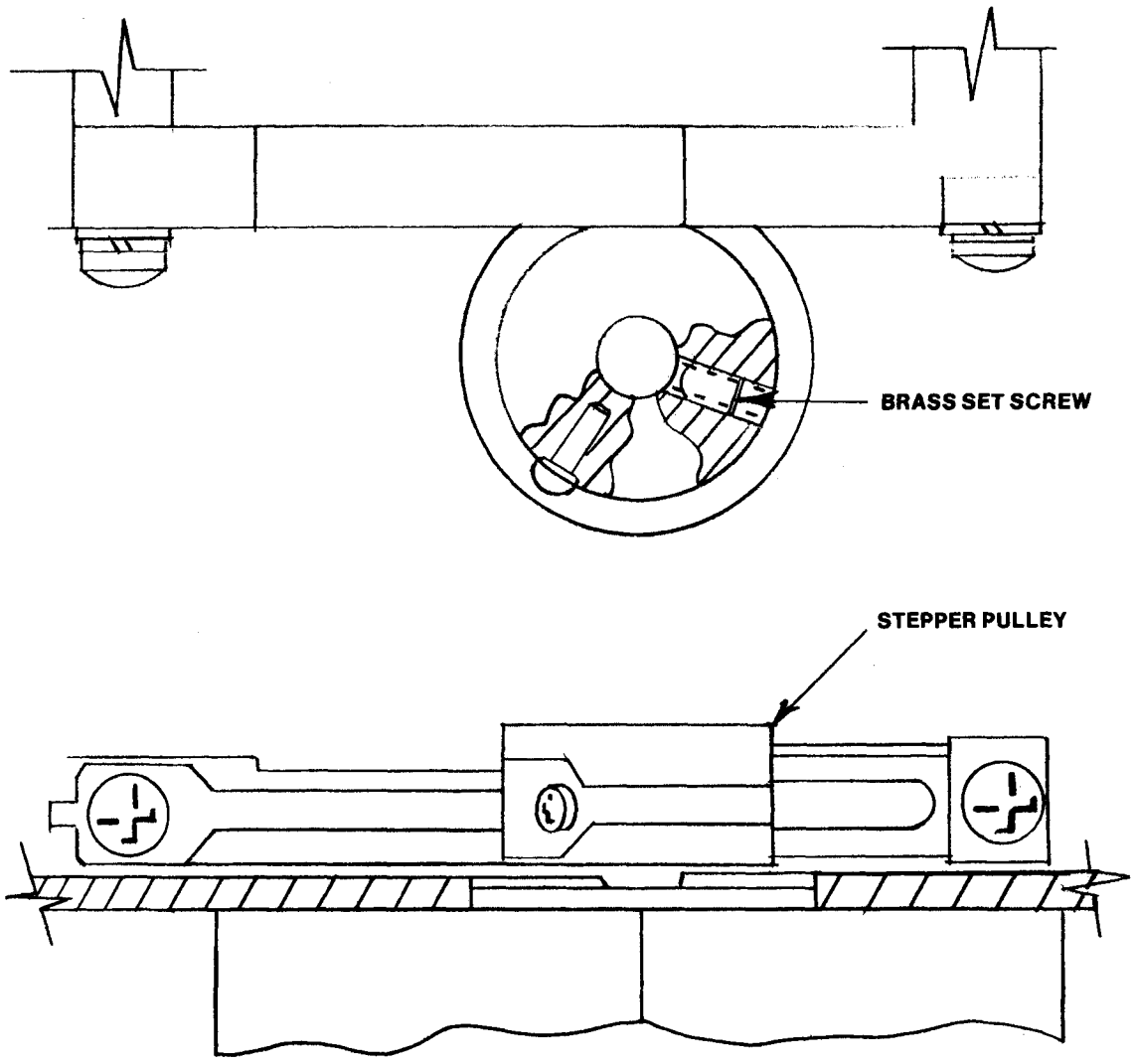


FIGURE 5-20 STEPPER PULLEY/BAND ASSEMBLY

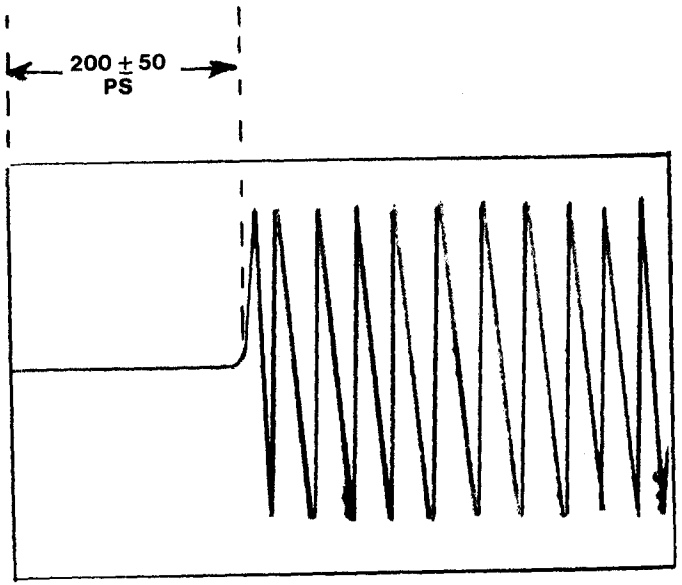


FIGURE 5-21 INDEX-TO-DATA ALIGNMENT PATTERN

5.2.4 Index-to-Data Alignment

1. Perform set up in paragraph 5.2.3.
2. Remove mounting plate.
3. Loosen the two index sensor mounting screws located at the back of the drive in the recessed area (see Figure 5-22).
4. Slide the sensor such that the scope shows a data pattern starting 200 $\pm$ 50 microseconds from the start of the trace (See Figure 5-21).
5. Tighten the screws carefully so that no variations in the scope display occur (20 inch-ounce).

5.2.5 Track 00 Sensor Check

1. Verify the radial-track alignment (see paragraph 5.2.1).
2. Apply power to the system and select drive.
3. Connect channel A probe to connector J4-12 (see Figure 5.17); set scope trigger to INTERNAL/AUTO; put ground probe to ground end of C30 or C31 (see Figure 5-18).
4. Check that the signal at J4-12 (blue connector) is 0.5V maximum at track positions of key 0, 1, and 2.
5. Check that the signal at J4-12 is +4.0V minimum at track position 03.
6. If voltages are not correct, perform the adjustment below.

5.2.6 Track 00 Sensor Alignment

1. Remove head connector (brown) from printed circuit board. (See figure 8.xx Photo IPB)
2. Remove printed circuit from mounting (2 screws).
3. Remove shield cover.
4. Perform the set up in paragraph 5.2.5.
5. Loosen the two track 00 sensor mounting screws (top/rear of disk drive). See Figure 5-23.
6. Adjust sensor so that the signal at J4-12 is 0.5V maximum at track positions of 00, 01 and 02.

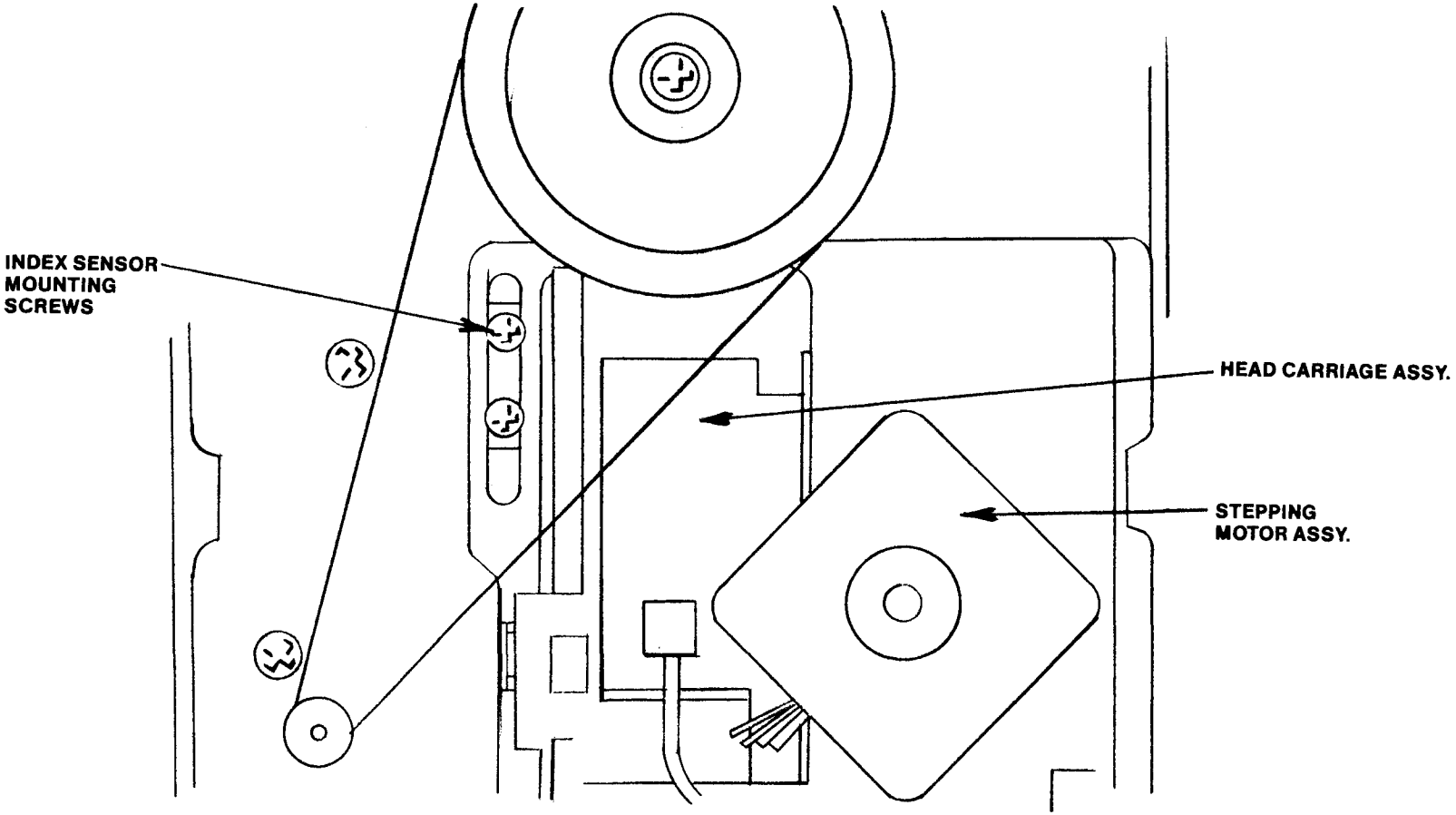


FIGURE 5-22 INDEX SENSOR MOUNTING SCREWS

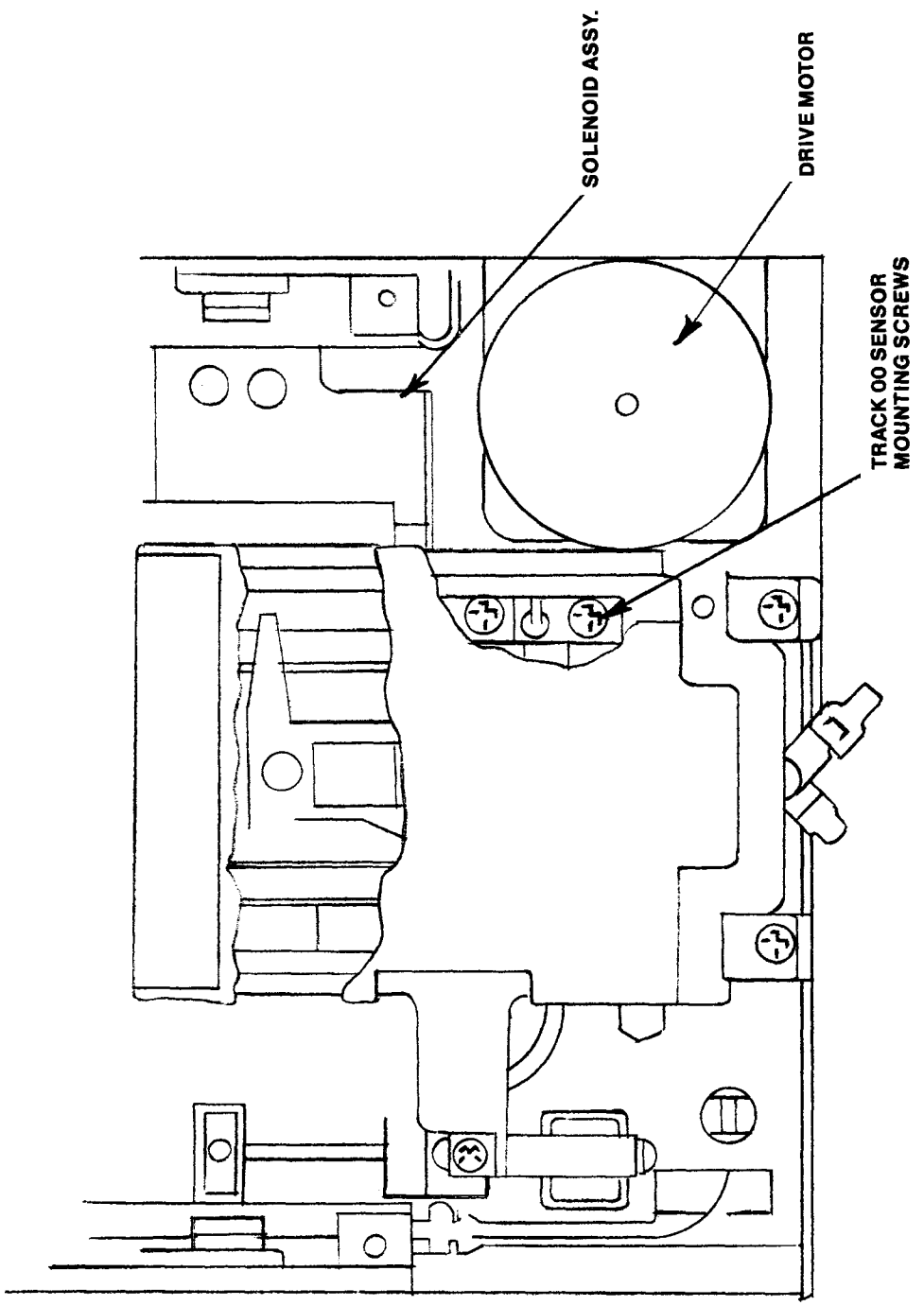


FIGURE 5-23 TRACK 00 SENSOR MOUNTING SCREWS

5.2.7 Speed Control Check

1. Remove mounting bracket.
2. Apply power to System 420 and select drive (option switch 8 ON).
3. Insert a diskette and close door.
4. Turn disk drive on its side and observe the strobe effect of spindle pulley.
5. If operating from 60 Hz power observe outer trace stability. If operating from 50 Hz power observe inner trace. If trace stability is unacceptable, perform the procedures in paragraph 5.2.8.

5.2.8 Speed Control Adjustment

1. Perform the set-up in paragraph 5.2.7.
2. Adjust R38 on disk drive PCB for a near stable or stable strobe pattern (see Figure 5.18).

NOTE:

A small amount of strobe creep is permissable.

5.2.9 Track 00 End Stop Check

1. Verify radial track alignment (see paragraph 5.2.1).
2. Verify the track 00 sensor alignment (see paragraph 5.2.5).
3. Apply power to the disk drive and select drive.
4. Command a seek to track 00 (key 0).
5. Check that a maximum track seek and a return to track 00 will cause the carriage to be within 0.010 inch/0.0254 cm of end stop (key 6 and key 0).
6. If carriage is not within specifications (0.010 inch/0.0254 cm), perform adjustment in paragraph 5.2.10.

5.2.10 Track 00 End Stop Adjustment

1. Perform set up in paragraph 5.2.9.
2. Adjust the set screw located on the left-hand boss in the rear of the drive to approximately 0.010 inch/0.0254 cm from the end of the carriage (approximately one-half revolution of the set screw).
3. Verify adjustment by commanding a maximum track seek and a return to track 00. Be sure that the carriage does not hit the end stop (key 6 and key 0).

5.2.11 Neoprene (Block) Drive Belt Check

If the drive belt is too loose, adjust as described in paragraph 5.2.12.

5.2.12 Neoprene Drive Belt Adjustment

1. Loosen drive motor mounting screws on the bottom of the chassis (see Figure 5.24).
2. Position the drive motor as close to the spindle assembly as possible.
3. Tighten the drive motor mounting screws.

NOTE:
No belt tension measurement is necessary.

5.2.13 Check Ejector Latch and Ejector-Latch Release

Check that the ejector latch and the ejector-latch release are not deformed in shape. Any deformed parts should be replaced before adjustment is performed.

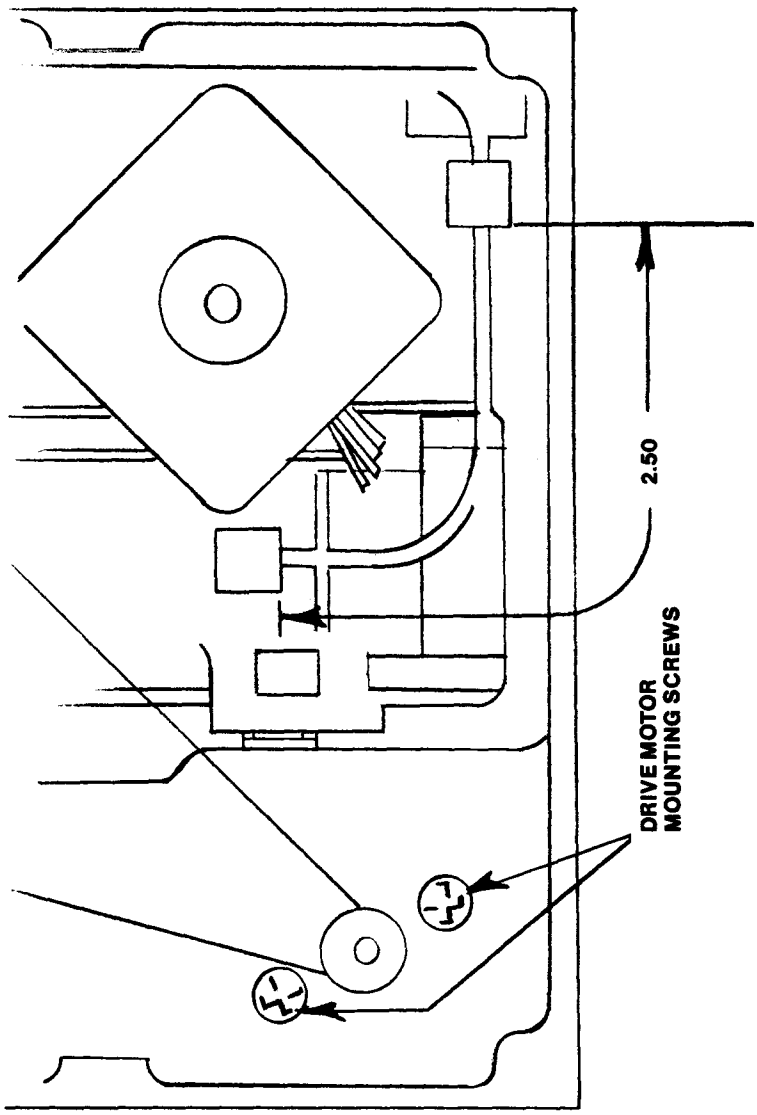


FIGURE 5-24 DRIVE MOTOR MOUNTING SCREWS

5.2.14 Ejector Latch and Release Adjustments

1. Remove ejector block and latch (see Figure 5.25).
2. After installing the ejector block and latch, center the "window" in the latch about the "tab" on the block (see A).

NOTE:
Do not tighten latch release screw.

3. With the ejector block in the latched position, close the door and install latch release (do not tighten latch release screw.)
4. Allow latch release to rest against front edge of latch (see C).
5. Position latch release at top/inside edge of carrier arm (or adaptor mounting block) (see B).
6. Tighten screw, making sure that the latch release does not rotate about the screw.
7. Open door -- latch should release.
8. Open and close door two or three times. The latch should slightly deflect and then be overridden by the latch release both in the opening and closing directions.

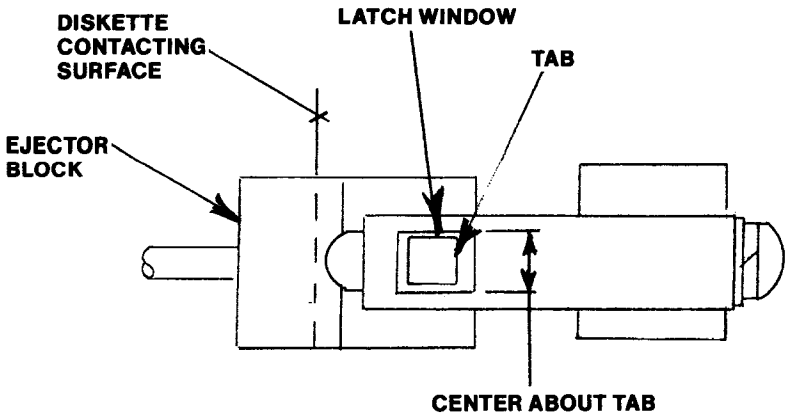
5.3 VIDEO MONITOR

CAUTION

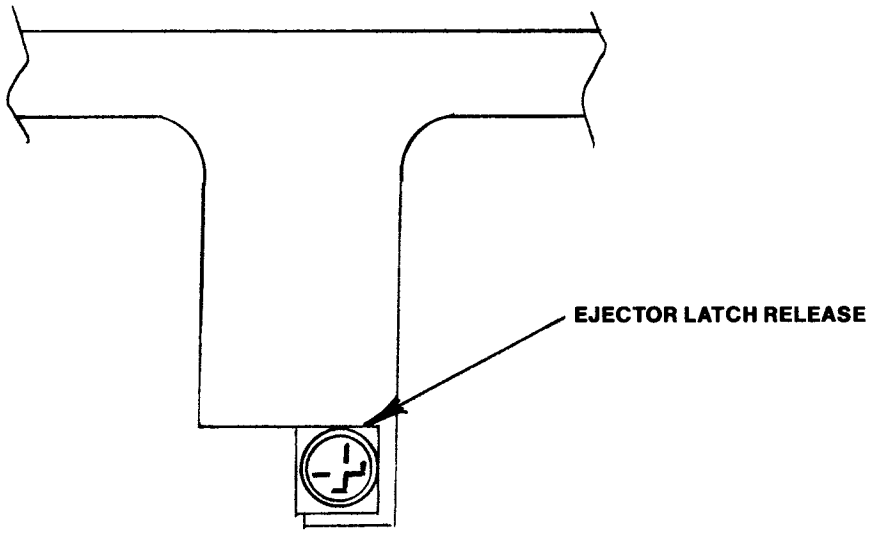
No work should be attempted on an exposed Video Display Chassis by anyone not familiar with servicing procedures and precautions.

SAFETY WARNING

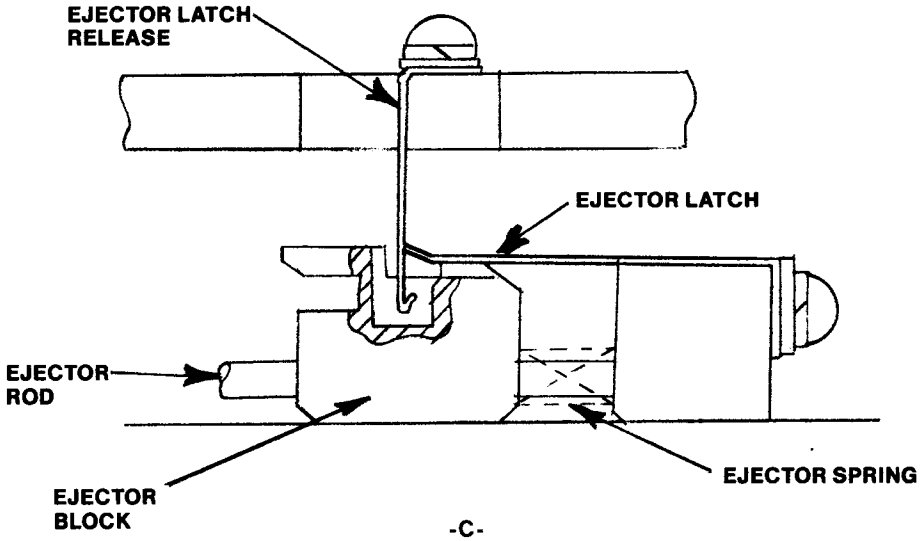
A good practice, when working inside any electronic chassis, is to use only one hand. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on a high voltage electrical connection, causing severe electrical shock.



-A-
EJECTOR BLOCK AND LATCH
-TOP VIEW-



-B-
CARRIER ARM
-TOP VIEW-



-C-
EJECTOR ASSEMBLY

FIGURE 5-25 THREE VIEWS OF EJECTOR ASSEMBLY

Extreme care should be used in handling the cathode ray tube; rough handling may cause implosion, due to atmospheric pressure. Do not nick or scratch the CRT or subject it to any undue pressure.

Avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger or personal injury from unnecessary exposure to X-ray radiation may result.

The alignment procedure for the CRT display is as follows:

CRT adjustments on the 7456 board such as focus, width, horizontal hold, phasing, vertical size, vertical linearity, and vertical hold are available from the monitor's pedestal when its front panel is removed (see Figure 5-26). The other board controls are factory adjustments.

5.3.1 Set-Up Screen: Create a document to display a full screen (80 by 24) filled with alternating characters "HO".

5.3.2 Horizontal and Vertical Hold Adjustments: Set both Horizontal hold (R33) and Vertical hold (R15) to middle of stable display range.

5.3.3 Vertical Height Adjustment: Adjust the vertical size (R24) for a vertical height of 8.5 inches, (21.6 cm) on the 12" display. (Use a standard or metric scale).

5.3.4 Vertical Linearity Adjustment: Adjust the vertical linearity (R18) for character rows of eaqual height. Repeat 5.3.3 and 5.3.4 until both requirements are met.

5.3.5 Screen Width Adjustment: Adjust the width coil (Z2) for 10 inches (25.4 cm) of horizontal deflection on the 12" display. (Use standard or metric scale.)

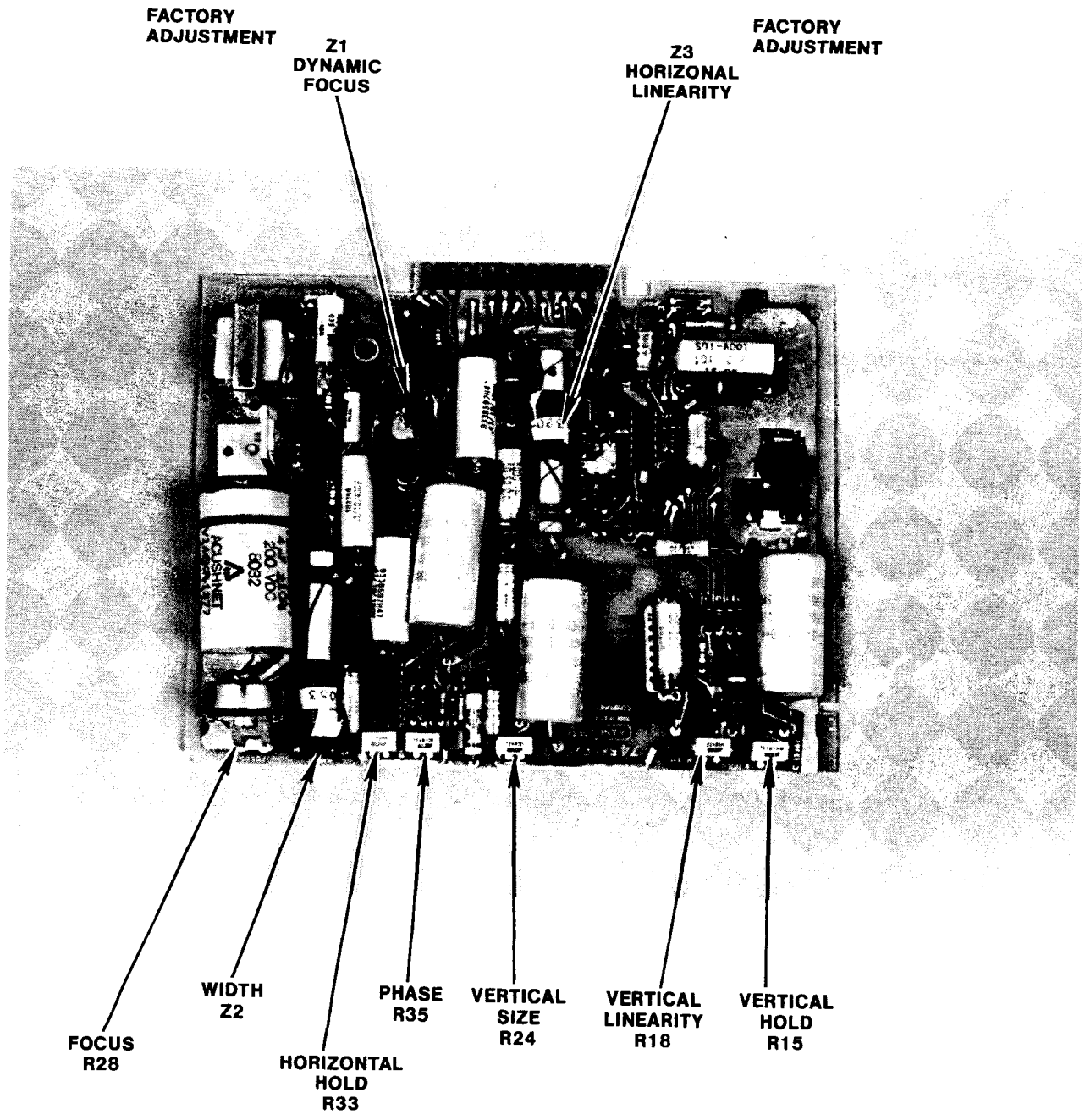


FIGURE 5-26 ELECTRONICS BOARD FOR 12-INCH DISPLAY MONITOR

5.3.6 Phase Adjustment: Adjust the phase adjustment (R35) for characters centered horizontal on the raster. (Turn the brightness up sufficiently to observe the raster frame.)

5.3.7 Focus Adjustment: Adjust the focus (R28) for the best overall screen display.

NOTE

See Reference Service Bulletin #73 for additional information on Wang CRT video display monitors (including factory adjustments).

5.3.8 PLL Check and Adjustment (VCO)

1. Turn sytem power OFF.
2. Remove right side (see Chapter 7 if necessary).
3. Remove printer PCA (see Chapter 7 in necessary).
4. Ground pin 24 (VCO sync) of L27 (UPD765) on CPU/disk PCA.
5. Put signal lead of scope (vertical input) to TP2 on CPU PCA.
6. Put scope ground lead to chassis.
7. Set Horizontal Sweep on scope to 0.2us.
8. Turn system power ON.
9. Adjust scope to obtain a 1us cycle time.
10. If the 1us cycle time is not present on scope, adjust pot in the lower-left corner of the CPU PCA.

NOTE

If unable to obtain waveform by adjusting the pot, replace CPU board.

11. Turn power OFF.
12. Remove ground at pin 24 of L27 on CPU/disk PCA.
13. Remove probe from TP2.
14. Remove scope signal and ground probes.
15. Replace printer PCA.
16. Replace right-side cover.

CHAPTER 6
PREVENTIVE MAINTENANCE AND DIAGNOSTICS

Preventive maintenance and diagnostics comprise respectively the periodic maintenance designed to optimize and extend equipment operation and the diagnostics used to isolate causes of equipment failure. The maintenance procedures included here consist of steps adviseable periodically regardless of the presence or absence of trouble symptoms; the system diagnostics compose a troubleshooting approach either to further define malfunctions detected by the power-up diagnostic or to isolate trouble sources not detected via other means.

6.1 PREVENTIVE MAINTENANCE

The recommended preventive maintenance consists of normal cleaning and inspection either every year, each 500 hours of operation, or present service call - whichever occurs first. The printer needs a visual inspection, cleaning, and minimal lubrication. Normal time required to perform these procedures should not exceed 15 minutes.

6.1.1 Cleaning and Inspection

1. Remove power from printer, and open or remove covers.

2. Inspect the printer for signs of wear and loose or broken hardware. Check the platen for looseness or wobble. Check the carriage system for looseness, wobble, or accumulations or foreign materials on the rail, which might cause uneven carriage movement. Check the carriage drive cable system for wear.

3. Remove the platen, paper cradle, ribbon cartridge and print wheel. Inspect these for signs of wear.

4. Clean the printer with alcohol-saturated cleaning pads and wipers. Remove accumulations of paper residue, ink, dust, etc., with special attention to carriage rails and pulley grooves. Heavy deposits may be first removed by a blast of compressed air.

5. Clean the platen, platen pressure rollers, and paper bail rollers with a good platen cleaner non-injurious to rubber products (such as Fedron Platen Cleaner). Do not use alcohol on these items.

6.1.2 Lubrication

Lubricate the various parts of the cleaned and inspected printer according to the following schedule. DO NOT exceed the amounts recommended. Oil should be #10 weight; grease should be IBM No. 23.

1. Clean both carriage rails with alcohol pads.

2. Carriage rail bearing: put 4 or 5 drops of oil on either side of the carriage, and move carriage back and forth.

3. With a cloth or brush, wipe away debris from the hammer actuator.

4. Remove the two caps from the hammer armature pivots, and apply grease on pivot pin. Do not oil the parts.

6.1.3 Check for Marginal Operation

Corrective steps, prompted by observed marginal operation of the equipment, may forestall emergency conditions. Printing characteristics to check are as follows:

1. Spacing: A row of uppercase "H"'s will show if any spacing problems are present in the machine.

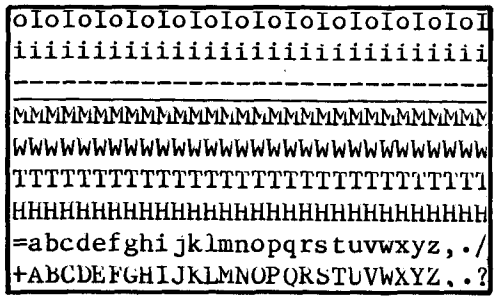
2. Typical Sentence: "The quick brown fox ..." This sentence uses all the alphabet in a random order.

3. Print Wheel Worst Case: I, E, H, X

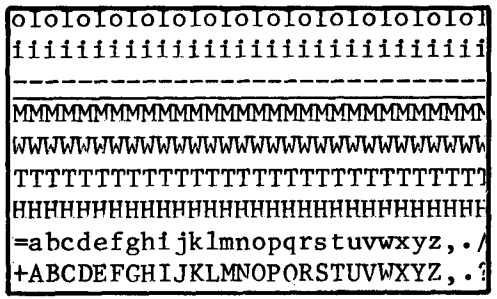
4. Line of under-scores.

5. Six line feeds equal to one inch.

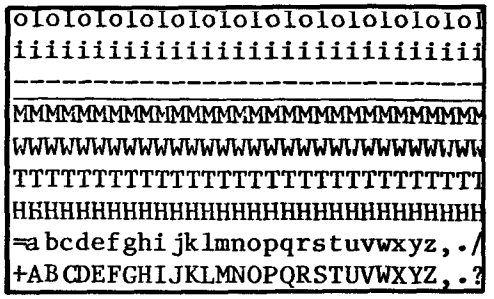
Refer to Figure 6-1 for the classifying of typical printer marginal operation.



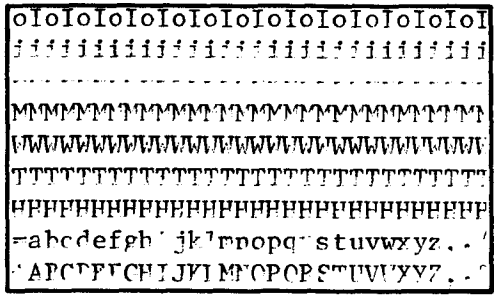
LETTERS TOO LIGHT AT TOP - EITHER PRINT WHEEL ADJUSTED TOO CLOSE TO PLATEN OR HAMMER ADJUSTED TOO HIGH



LETTERS TOO LIGHT AT BOTTOM - HAMMER EITHER TOO CLOSE TO PLATEN OR ADJUSTED TOO LOW

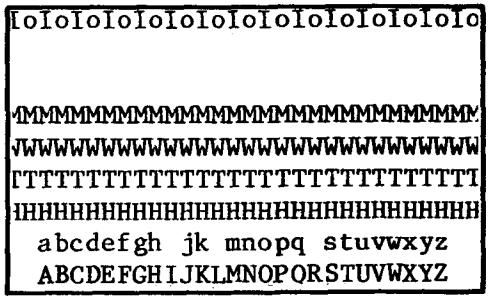


LIGHT PRINT - EITHER PRINT SOLENOID ARM-TO-LAMINATION GAP TOO SMALL OR HAMMER-TO-PLATEN GAP TOO GREAT

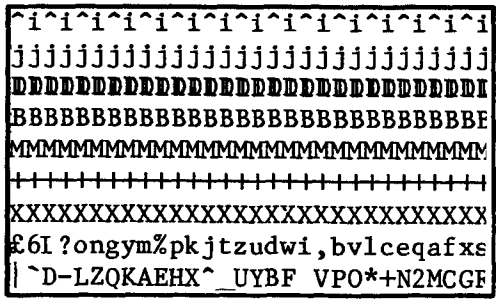


VERY LIGHT - PRINT WHEEL TO PLATEN GAP TOO GREAT

PROPER ADJUSTMENT



SMALL CHARACTERS NOT PRINTING - PRINT SOLENOID ARM-TO-LAMINATION GAP TOO LARGE



LETTERS OUT OF ALIGNMENT - HOME POSITION TOO FAR RIGHT, "0" TWO CHARACTERS TO THE RIGHT

FIGURE 6-1 PRINTER ADJUSTMENTS

6.2 SYSTEM DIAGNOSTICS

The system diagnostics consists of eight programs selectable either singly or in combination with one another as follows:

NAME (REVISION)	HARDWARE TESTED
Main Memory (1110)	Main memory starting at 4000 (hex)
CRT Memory (1110)	CRT memory excepting soft character generation
Z80 Instruction Set (1110)	CPU chip internal hardware
CTC (1110)	CTC (on the CPU/disk board)
Disk (1110)	Disk controller and disk drive
Display & Keyboard (6000)	CRT attributes, soft character memory, keyboard logic and keys
Lamp & Status (6110)	Printer switches, lamps, sensors, character counter; 7-segment display; device type (IN07) switch bank
Printer (0000)	Printer control logic

To initiate the system diagnostics:

1. Turn on the system power, then insert the program diskette. The program-selection menu should appear on the monitor.

2. When the program-selection menu appears, position the cursor by means of:

   up/down arrows
   space bar (=down)
   BACK SPACE (=up)

   (Choice of up/down arrows versus space bar/BACK SPACE control is optional)

3. Select, or deselect, programs by means of:

   INSERT - for selection
   DELETE - for deselection

4. Key EXECUTE to initiate the selected test(s). An instructional/ informational diaplay (run-time menu) should appear on the monitor (except when the display and keyboard test is selected; see paragraph 6.2.6) as follows:

```
INDENT = Error Loop     PAGE   = Routine Loop   CENTER = Stop on Error
DECTAB = Program Loop   FORMAT = Pause          MERGE  = Scope Loop
STOP   = Clear All Settings

Program Name:                       Program Status     :
Routine Name:                       Program Set Count  :
Error Code  :                       Routine Loop Count :
Error Count :                       Program Loop Count :

                                    Keyboard Status    :

Messages:
```

The uppermost portion of the run-time menu display composes a quick-reference summary of the special meanings assumed by certain control keys when under system diagnostic program control. Command functions thus enabled by the controlled keys are as follows (function key names are in parentheses):

- Error loop (INDENT) - Loop on routine in which the next failure occurs.
- Loop on Program (DECTAB) - Loop on current diagnostic program.
- Pause (FORMAT) - Halt the program.
- Test Loop (PAGE) - Loop on current test routine.
- Clear all Settings (STOP) - Stop looping, if looping, or resume testing if halted.
- Scope Loop (MERGE) - Loop on next test routine in which a hardware failure occurs.
- Stop on Error (CENTER) - Stop the diagnostic program where the next failure is detected.
- Error Log (COMMAND) - Display the error log screen. Use NEXT SCRN to return to the run-time menu and clear the error log. Use PREV SCRN to return to the run-time menu and save the error log.

Immediately below the switch function summaries, the run-time menu displays a group of category headings (test descriptors) tallying various operational aspects of the test currently in progress as follows:

Program Name - test name currently in progress

Routine Name - current routine within test currently in progress

Error Code - the number of the most recently detected error

Error Count - Cumulative error count - cleared by a return to the program selection manu

Program Status - current operation in progress, e.g., test in progress, program paused, etc.

Program Set Count - count of the number of loops made through the set of programs - cleared by a return to the program selection menu

Routine Loop Count - count of the number of loops made through the current routine

Program Loop Count - count of the number of loops made through the current program

Keyboard Status (locked/unlocked) - indicates whether keystrokes are to be accepted when made (unlocked), or whether acceptance is to be delayed. If a key is struck while the keyboard is locked, the struck key highlights until accepted. During this (locked) period, the unit ignores subsequent keystrokes, i.e., does not store more than one.

The test program currently being performed writes error messages and user prompts in the lower half of the run-time menu. If more than one error occurs, only the last error message is left on display, although the error count increments for each error.

The selected diagnostic programs run (when EXECUTE is keyed) in the order shown on the program-selection menu. If testing is altered neither by operator action nor by hardware failure, the monitor automatically repeats the set of selected diagnostic programs. Keying CANCEL causes the monitor to redisplay the program-selection menu.

6.2.1 Main Memory Diagnostic

The main memory diagnostic consists of:

TEST NO.	TEST NAME	HARDWARE TESTED
01	Bank Addressing	Bank address and page select lines
02	Chip Addressing	Chip address lines
03	Moving Inversion	Memory data

The tests run in the order as listed above; once started, the program runs either until down or until an error is detected. The amount of memory tested depends upon the settings of the switch bank on the CPU board:

Switch 1	Switch 2	Memory Size
OFF	OFF	48K
OFF	ON	64K
ON	OFF	80K
ON	ON	96K

All error messages will begin in this form:

(type of error) at (address) and page xx
Received data = xx
Expected data = yy

The important details of this message are in the address of the fault, and the page number. The address enables the user to determine which bank of chips contains the fault (see table below), the page number indicates one of the banks at location 8000 (hex).

Bank #	Page #	Address
0	N/A	0000-3FFF
1	N/A	4000-7FFF
2	0	8000-BFFF
2	1	8000-BFFF
2	2	8000-BFFF
2	3	8000-BFFF

In the case of addressing errors, the failing address line(s) are identified, along with the apparent type of failure (stuck, open or shorted address line(s)). In most cases, only the open address lines can be fixed in the field.

Error	Error Type	Suggested Repair Action
01	Data Error	Replace Memory Chip(s) or Board
02	Data Error	Replace Memory Chip(s) or Board
03	Bank address(short, open)	Replace Memory Board
04	Pages Bank address(short, open)	Replace Memory Board
05	Chip address (short, open)	Replace Memory Chip(s) or Board
06	Chip address (stuck)	Replace Memory Board

6.2.2 CRT Memory Diagnostic

The CRT memory diagnostic tests addressing and data reliability on all of CRT memory, excepting the soft character font. The diagnostic comprises the following tests:

Test No.	Test Name	Hardware Tested
01	Bank Addressing Test	Bank address and page select lines
02	Chip Addressing Test	Chip Address lines
03	Moving Inversion Test	Memory data test

Once started, the program runs either until done or until an error is detected.

6.2.3 Z80 Instruction Set

The Z80 instruction set test checks execution of all the instructions in the instruction set. The test verifies operation of hardware internal to the chip, consisting of the following:

The accumulator with logic and rotate commands
3-bit multi-purpose registers
The remainder of the rotate and shift commands
The 16-bit register pairs using indirect addressing
The exchange commands
Index registers
The stack pointer
The push and pop commands
The arithmetic group
The bit test group
The compare and block transfer group
The call and set commands
The indexed addressing mode

The test performs each instruction at least once; an error check occurs at each stage during the test of an instruction. The test generates an error message if the data and/or flags are incorrect.

6.2.4 CTC Diagnostic

The CTC diagnostic tests the CTC chip and interrupt circuitry on the 7777 CPU board. The tests are as follows:

Test No.	Test Name	Hardware Tested
1	Timer Mode	CTC, CPU Interrupt logic
2	Interrupt Priority	CTC interrupt daisy chain, CPU interrupt logic

Once started, the program runs either until done or until an error is detected.

6.2.5 Disk

The disk test checks the disk controller circuitry on the CPU/disk board, and checks the disk drive and cable. The tests are as follows:

Test No.	Test Name	Hardware Tested
1	Disk Reset	FDC (floppy disk controller), PIO
2	Disk Ready	FDC, ready signal
3	Track Zero	FDC, track zero signal
4	Cylinder Addressing	FDC, seek circuitry on drive
5	Forward Seek	FDC, seek circuitry on drive
6	Backward Seek	FDC, seek circuitry on drive
7	Format	FDC, disk drive
8	Read/Write	FDC, VCO, disk drive

If switch 4 on the CPU board is positioned on (indicating presence of two disk units in the system), the message portion of the run-time menu states the options available for testing disk units 0 and 1 as follows:

0: To test unit 0, hit the 0 key, then hit EXECUTE
1: To test unit 1, hit the 1 key, then hit EXECUTE
2: To test both units 0 and 1, hit the 2 key, then hit EXECUTE

If switch 4 is positioned off, unit 1 is effectively the only drive in the system; the test selects unit 1 automatically.

Following selection, either manually (should two disk units be in the system) or automatically (if but one disk unit), the menu calls for insertion of a scratch diskette into each unit under test. A depressing of EXECUTE starts the test.

If disk unit 1 has been selected (either singly or in conjunction with unit 0), an end-of-test message instructs the operator to remove the scratch diskette from unit 1, to re-install the diagnostic diskette, and to depress EXECUTE (unless the loop on program option is in effect, in which case the end-of-test message does not appear).

6.2.6 Display and Keyboard Diagnostic

The display and keyboard test checks elements of the keyboard, and the CRT/memory and CPU/disk boards. The tests are as follows:

Test No.	Test Name	Hardware Tested
1	Display Attributes Test	Attribute logic, CRT/memory board, and associated logic, CPU/disk board
2	Keyboard Test	Keyboard assembly and keystroke logic on CRT/memory board
3	Soft Character Generator Test	Soft character generator memory on CRT/memory board and support elements on CPU/disk board

Unlike the other tests composing the system diagnostics, the display and keyboard test generates display patterns instead of a menu. For test and experimental purposes, some parts of the tests call for operator action.

Display Attributes (Figure 6-2)

The display attributes test generates a multi-line display. Each of the first nine lines shows the effect of turning on one attribute only. The next to last line (SCRIPT COMPARISON) sequentially invokes subscript, then no attribute, then superscript, then double superscript in order to produce the effect of a smoothly rising line of characters. The line then moves smoothly down to produce an overall effect of a wavy line. The last line shows various characters generated by the soft character memory.

Application of the various attributes progresses repetitively across the display, left to right. Figure 6-2, A and B, shows the sweep as having progressed respectively part way and full way across the display.

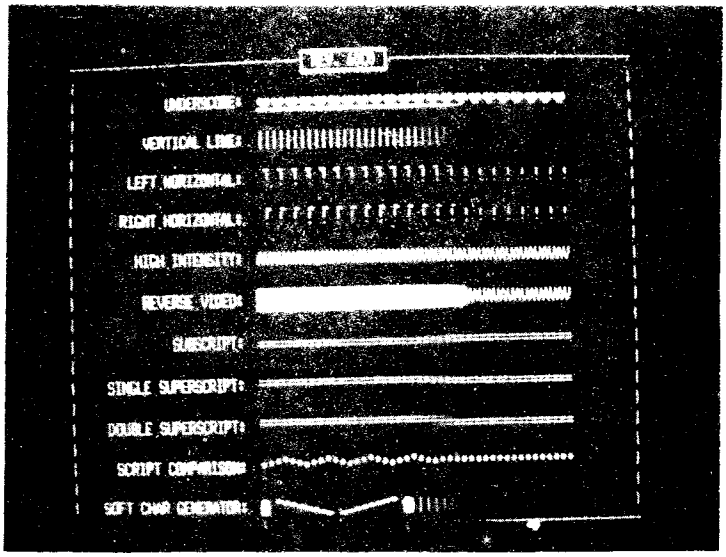
To perform the test:

1. Observe that all attributes affect the display as called for by the pattern.

2. Observe that all dots within the matrices displayed from the soft character generator both turn on and turn off within the various patterns.

3. Exit from the test by depressing (simultaneously) the shift key and CANCEL.

A



B

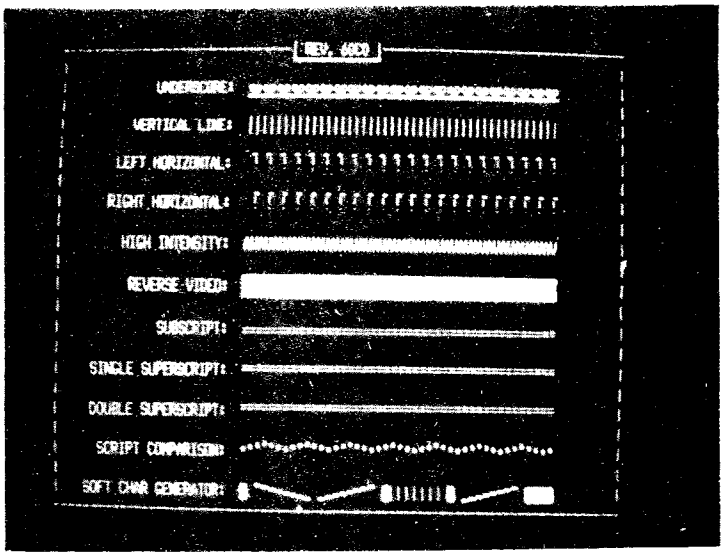


FIGURE 6-2 DISPLAY ATTRIBUTES

Keyboard Test (Figure 6-3)

A depressing of the shift and CANCEL keys (or any unshifted key) during the display attributes test initiates the keyboard test. The keyboard test causes a representation of the keyboard to be displayed. Performance of the test requires operator action as follows:

1. Depress twice the firt key to be highlighted (uppermost left) in the display. The next adjacent key to the right should highlight.

2. Repeat step 1 for each subsequent highlighted key throughout the display (note that in some instances, a simultaneous depressing of the shift key is indicated).

If an incorrect keystroke is detected, the key that corresponds to the incorrect keycode flashes, and an error message displays as shown in Figure 6-3. If the incorrect keycode does not correspond to an existing key, no key flashes; however, the data line is displayed.

Soft Character Generator Memory (Figure 6-4)

A depressing of the shift and CANCEL keys during the keyboard test initiates the soft character generator memory test. The soft character generator memory test causes a display of sixteen character spaces, each space labeled to permit determination of the respective memory addresses thus represented. Until modified by keystroke, the generator writes the dedicated portion of memory with alternate entries of all F and all 0; the visual effect should be that of 128 rectangles alternating every 5 seconds with 128 blanks.

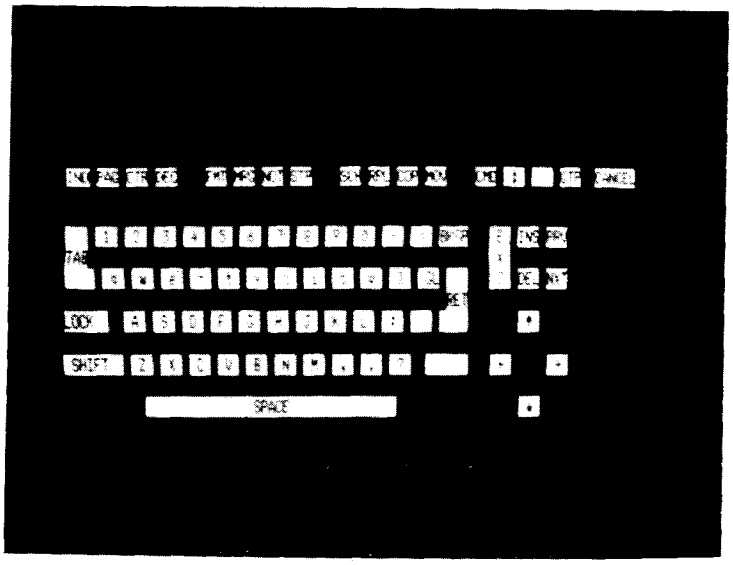


FIGURE 6-3 KEYBOARD TEST

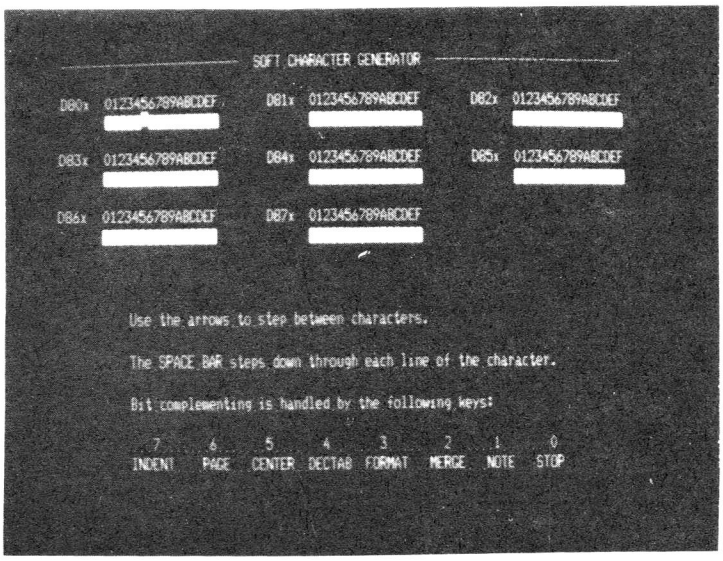


FIGURE 6-4 SOFT CHARACTER GENERATOR MEMORY TEST

The alternating displays permit a check to determine that no bits (dots) stick in either the on or off state. To toggle individual bits manually (for diagnostic purposes), perform the following:

1. Depress any key other than shift-CANCEL to freeze the display (preferably when the rectangles are on rather than blanked). The display double superscripts the upper leftmost rectangle to indicate selection for modification. Use of the cursor control arrow keys selects other rectangles for modification (see Figure 6-4).

2. Successively depress the leftmost seven command keys at the top of the keyboard to toggle the seven bits in a given line in the selected rectangle. One line in the selected rectangle should blank out.

3. To select other lines within the selected rectangle, depress the space bar. Each depressing of the space bar selects the next lower line, cycling back to the top line following selection of the bottom line.

4. To terminate the test, depress shift-CANCEL.

6.2.7 Lamp and Status Diagnostic

The lamp and status diagnostic tests:

- Printer panel switches, lamps sensors, character counter
- Seven-segment display
- Slave type (IN07) switch bank
- Associated cables

The test creates a screen display (shown below) which shows the condition of printer switches and sensors, and of the slave type switch bank. The program requires operator intervention and observation. Depression of a given switch, and observation of effects on the menu, establishes switch functional status.

MESSAGE AREA OF THE MONITOR

Panel Switches	SEL	RU	RD	FU	FD	TOF	PL
	ON	OFF	OFF	OFF	OFF	OFF	OFF
Status Switches	RM	LM	RO	PO	CO	DH	
	OFF	OFF	OFF	OFF	OFF	OFF	

Slave Type Switch 0 0 1 0 0 0 0 0
(Bits 1 2 3 4 5 6 7 8)

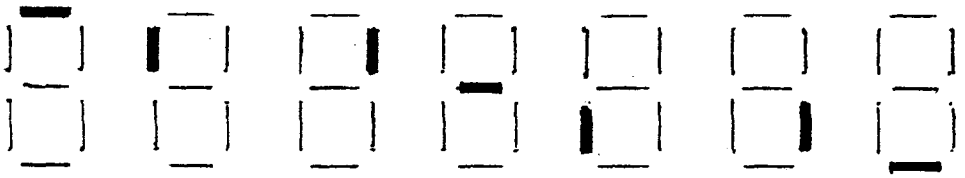
The abbreviations used in the Panel Switches section of the menu indicate switch and associated indicator as follows:

Panel Switch Name	Menu ID	Associated Indicator
Select Key	SEL	Select Lamp
Roll Up	RU	Change Ribbon Lamp
Roll Down	RD	Change Paper Lamp
Line Feed Up	FU	Error Indicator
Line Feed Down	RD	Change Daisy Lamp
Top of Page	TOF	Character Counter
Paper Load	PL	N O N E

The OFF/ON menu indication refers to the expected condition of the associated indicator. Thus, the ON shown below the SEL in the menu indicates that the select lamp should be lighted, etc. Each time a panel switch is depressed, with the exception of the TOF and FU switches, both the indicator and the associated menu representation should change condition from off to on and vice versa.

The TOF switch controls the character counter at the rear bottom of the unit. Each depression of the TOF switch should increment the counter by one.

The FU switch controls the seven-segment error display at the rear of the unit. Successive depressions of the FU switch first blank the display, then light individual segments in the following sequence.



The abbreviations used in the Status Switches section of the menu indicate respective associated sensors as follows:

Sensor Name	Sensor Menu Id Code
Right Margin	RM
Left Margin	LM
Ribbon Out	RO
Paper Out	PO
Cover Open	CO
Daisy Home	DH

The blocking of a given sensor by either an opaque or a reflective material causes the menu to display an on condition for the associated status switch; an unblocked sensor results in an off indication.

The Slave Type Switch section of the menu displays either a 1 or a 0 indicating respectively either an off or an on condition at the given position (as shown on the plastic case of the switch bank).

CHAPTER 7

REMOVAL AND REPLACEMENT

Equipment to be replaced may be removed in accordance with the procedures and illustrations contained in this chapter.

7.1 SIDE COVERS REMOVAL

1. In back of console, remove both the video and keyboard cables (see Figure 7-1).

2. Lift printer transparent protective hood.

3. Lift right and left side flaps.

4. Loosen the two large screws (1) on the inside left and right sides of the printer compartment (see Figure 7-2) until the sides are free.

5. Slide the side covers off.

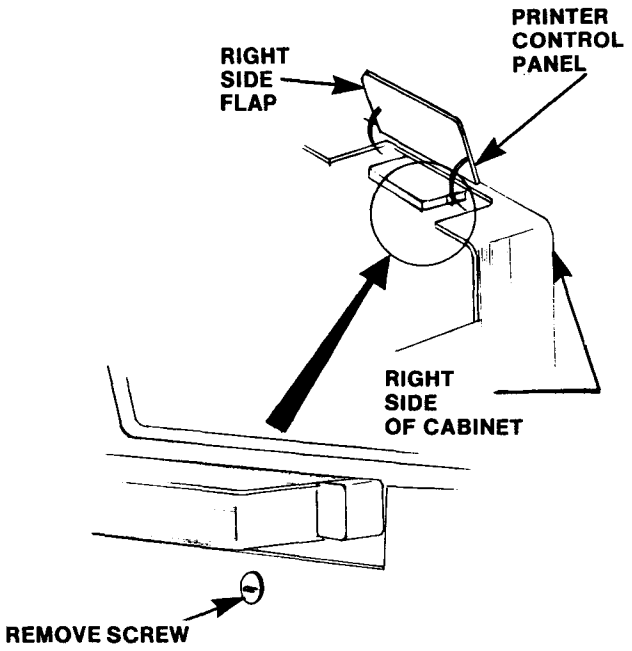


FIGURE 7-2
RIGHT SIDE COVER REMOVAL

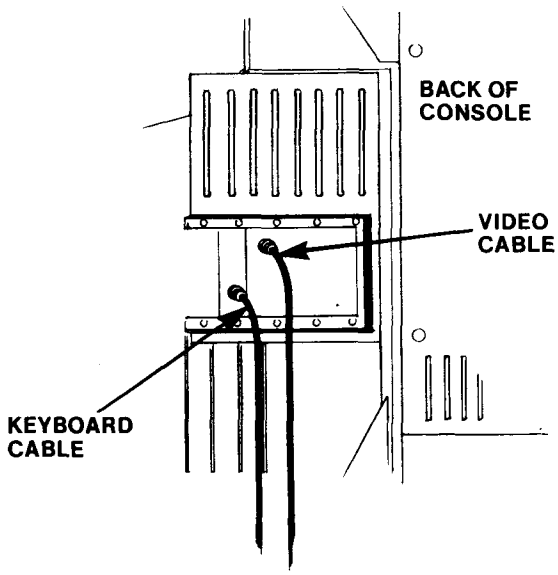


FIGURE 7-1
KEYBOARD & VIDEO CABLES

7.2 PRINTER REMOVAL

1. Remove side covers as described in paragraph 7.1.

2. Remove the two screws (on outside of frame) that hold the printer's control panel.

3. Disconnect the flex cable, motor power cable, paperfeed motor cable, and sensor cable from the 7776 PCA (see Figure 7-4).

4. Release the four printer legs from their shock mount by pulling up on each end of the printer unit one at a time.

CAUTION

DO NOT PULL ON CARRIAGE RAILS.

5. Lift printer out of console.

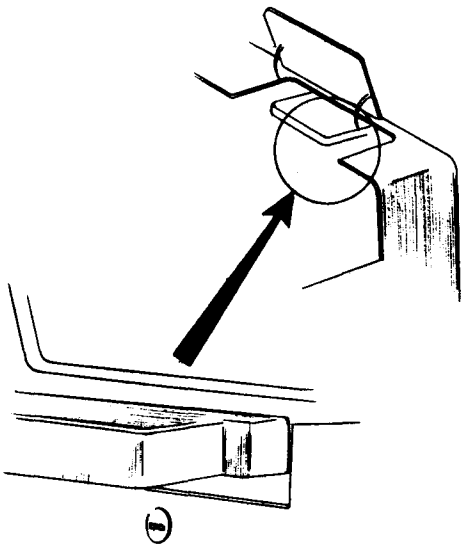


FIGURE 7-3
CONTROL PANEL REMOVAL

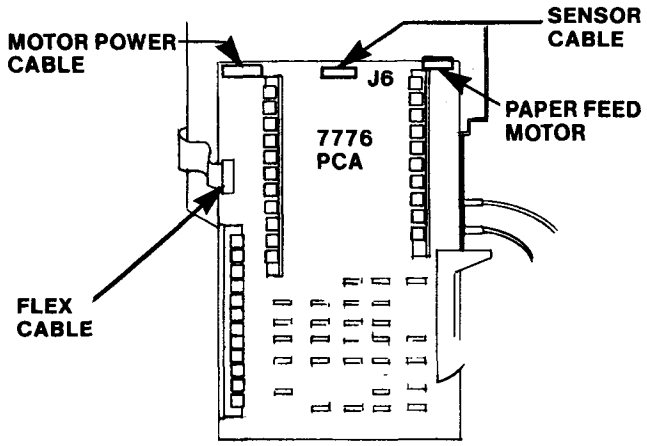


FIGURE 7-4
FLEX AND SENSOR CABLES

7.3 CPU, PRINTER AND CRT/MEM PCA REMOVAL

1. Remove the right side cover. Refer to paragraph 7.1

2. Remove the six (6) mounting screws that hold the metal brackets to the unit on the rear side of the PCAs (see Figure 7-5).

3. Remove the three (3) nuts (in front of PCA) that hold the boards to PCA support rods (see Figure 7-6).

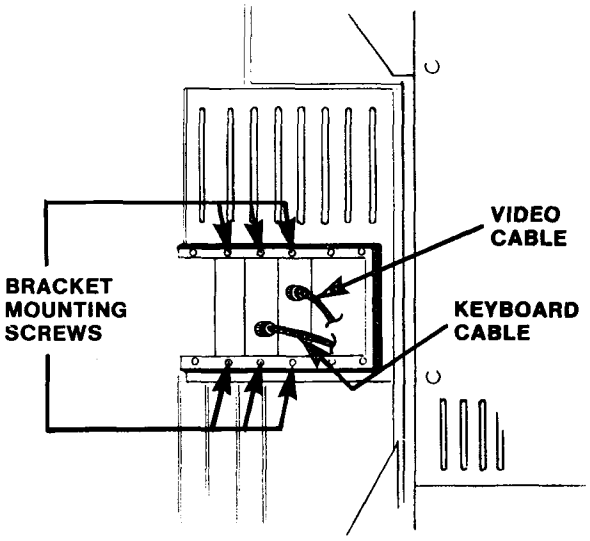


FIGURE 7-5
REMOVAL OF MOUNTING SCREWS

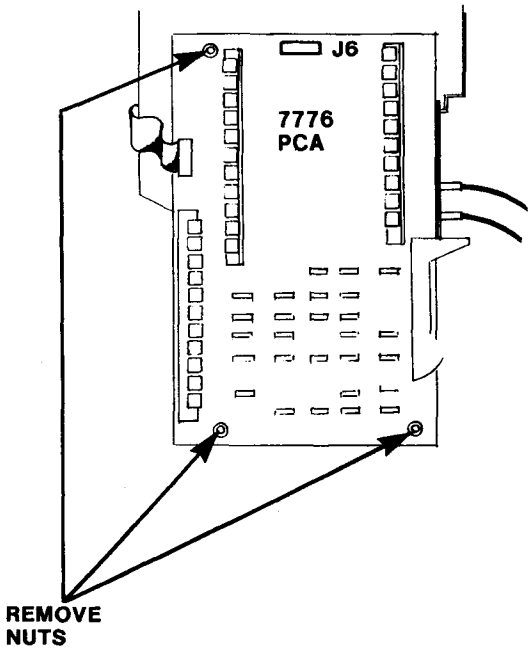


FIGURE 7-6
BOARD-TO-SUPPORT ROD NUTS

NOTE

The printer PCA is on the outside of cage. The CPU PCA is in the middle, and the CRT/-Memory is on the inside. Please note which connectors go where as you disconnect them. Also be careful of the seating of all connectors, especially the ZIF connectors.

4. Disconnect cables (see Figure 7-7 and Figure 7-8). ZIF connectors are released when the lever is pulled, as shown, on the PCA behind the PCA to be removed.

5. Remove PCAs.

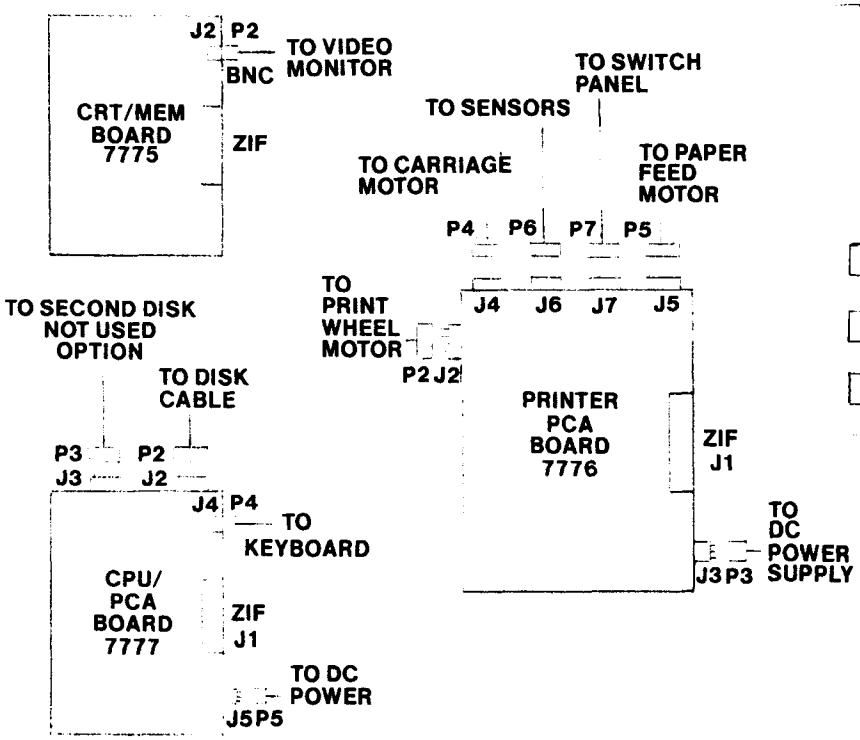


FIGURE 7-7
PCA CONNECTORS

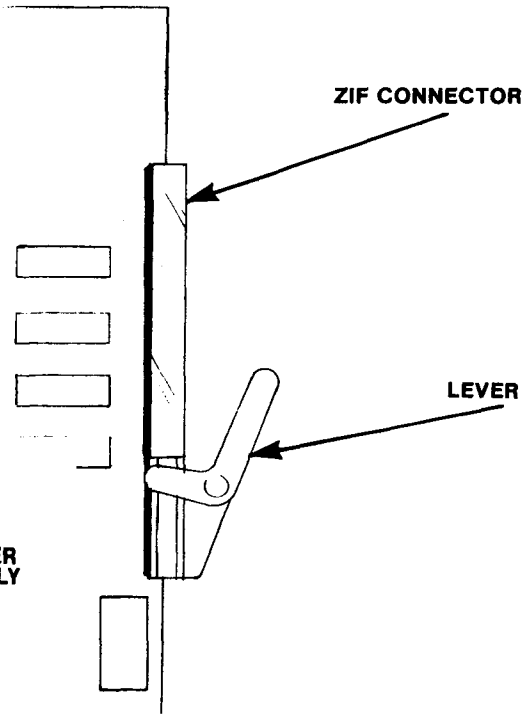


FIGURE 7-8
ZIP CONNECTOR

7.4 DISK DRIVE

1. Remove left side cover as specified in paragraph 7.1.

2. Disconnect both the ribbon cable and the power cable that go to the disk drive (see Figure 7-9).

3. Loosen the four mounting screws on the drive (see Figure 7-10), and slide the drive so the screws line up with the large holes at the end of the slots on the mounting bracket.

NOTE

Remove upper right screw only.

4. Remove disk drive.

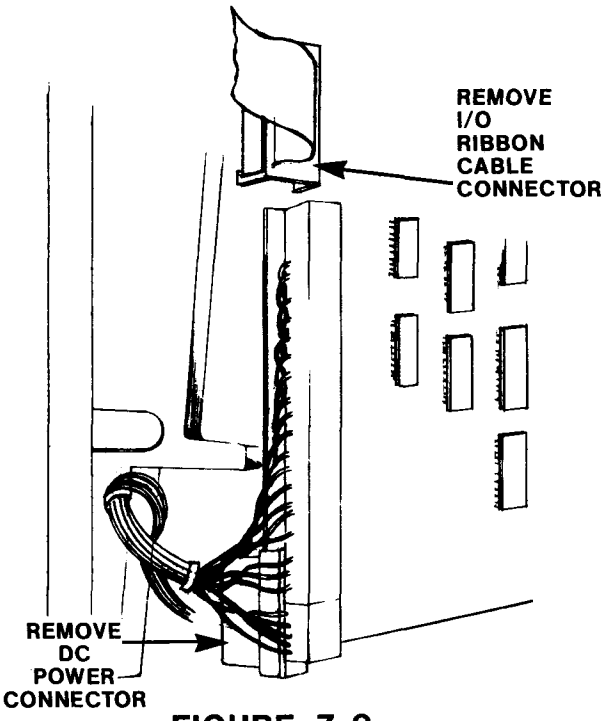


FIGURE 7-9
POWER AND RIBBON CABLES

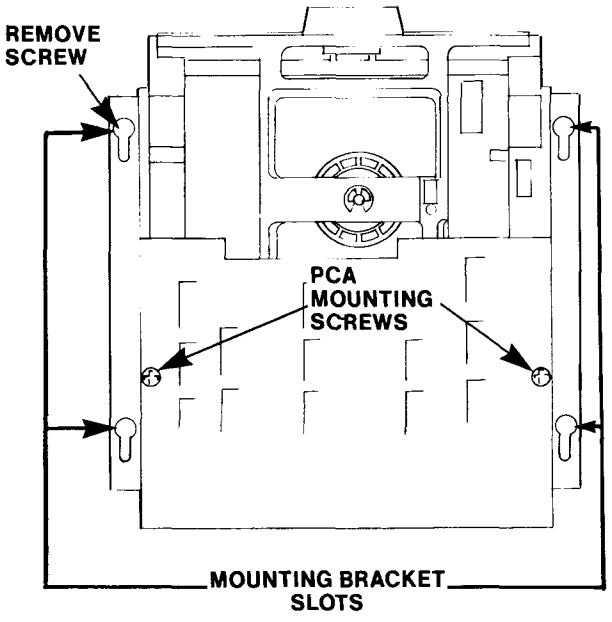


FIGURE 7-10
MOUNTING BRACKET SLOTS

7.5 REMOVAL OF FLOPPY PCA

1. Remove left side cabinet cover (refer to paragraph 7.1).

2. Remove the I/O and DC power connectors from the PCA (see Figure 7-9).

3. Remove connectors P4-1, P4-2, and P4-3 at right rear of PCA (see Figure 7-11).

4. Remove screws (2) at each side of the PCA (see Figure 7-10).

5. Pull PCA slightly to the rear of the disk drive.

6. Remove head connector(s) below and at left front edge of PCA. (Grip the connector(s), not the cables, when removing.) See Figure 7-11.

7. Slide PCA out the rear of the disk drive.

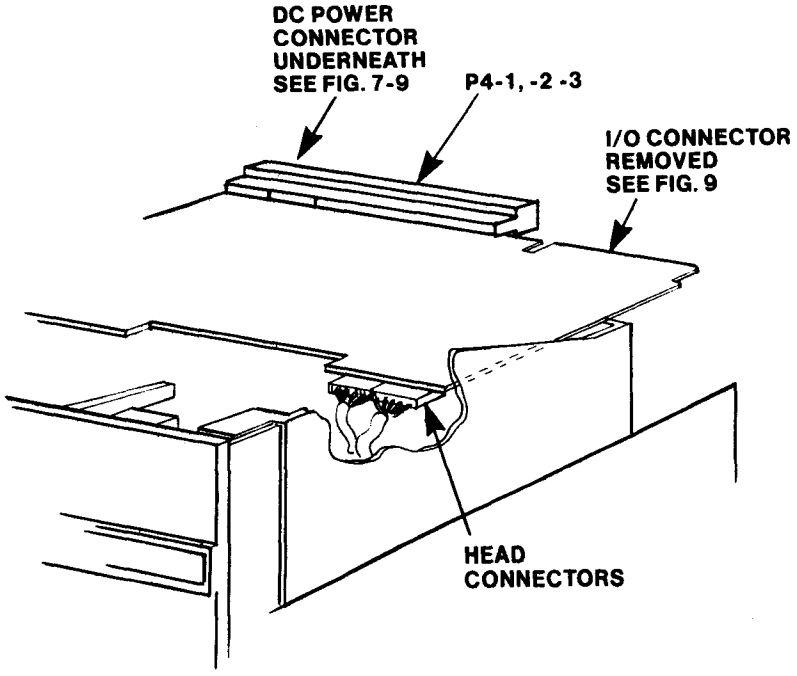


FIGURE 7-11
DISK PCA CONNECTORS

7.6 PRINT HEAD ASSEMBLY

1. Disconnect the head cable from the flex cable after releasing locking tab securing the connector (see Figure 7-12).

2. Release spring holding carriage base plate to front shaft bearing at copy control lever cutout.

3. Pull print head assembly forward and remove four (4) screws holding the assembly to the rear shaft bearing assembly. (Use care not to lose the shim between the carriage plate and bearing. See Figure 7-13.)

4. Lift head assembly from the printer unit.

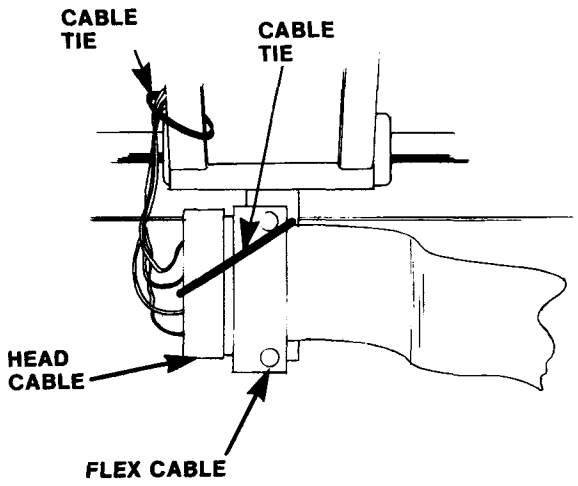


FIGURE 7-12 HEAD AND FLEX CABLE

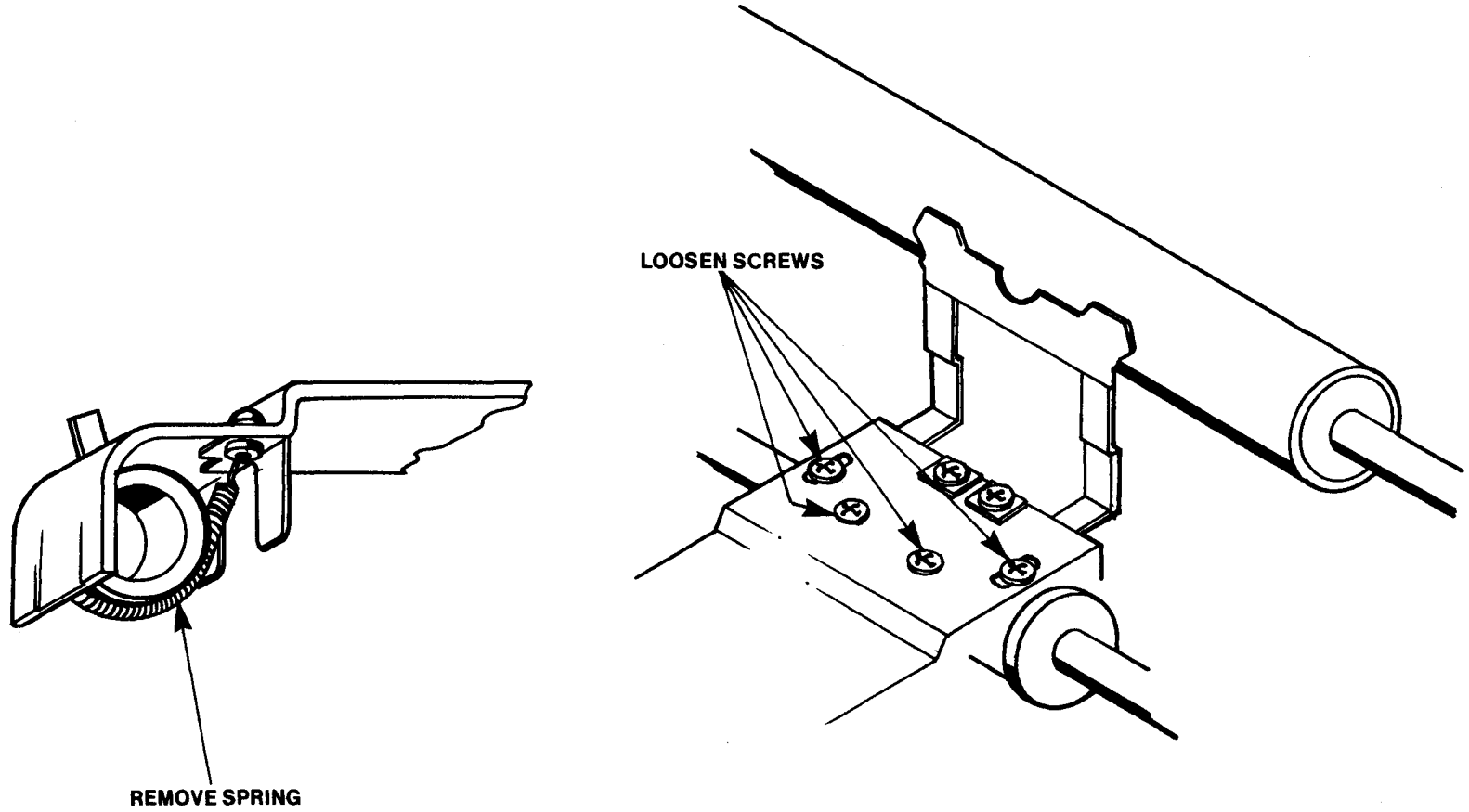


FIGURE 7-13 HEAD ASSEMBLY BASE PLATE MOUNTING

7.7 POWER SUPPLY

1. Remove AC power cord and power cable to CRT.

2. Remove side covers.

3. Remove the two screws on each side of the power supply (see Figure 7-14).

4. Remove cables on the printer driver board (P3 on left side).

5. Remove power cable to CPU board (P5 on left side).

6. Remove power-to-disk drive cable (P2 right hand side).

7. Slide the power-supply drawer out of the rear of cabinet.

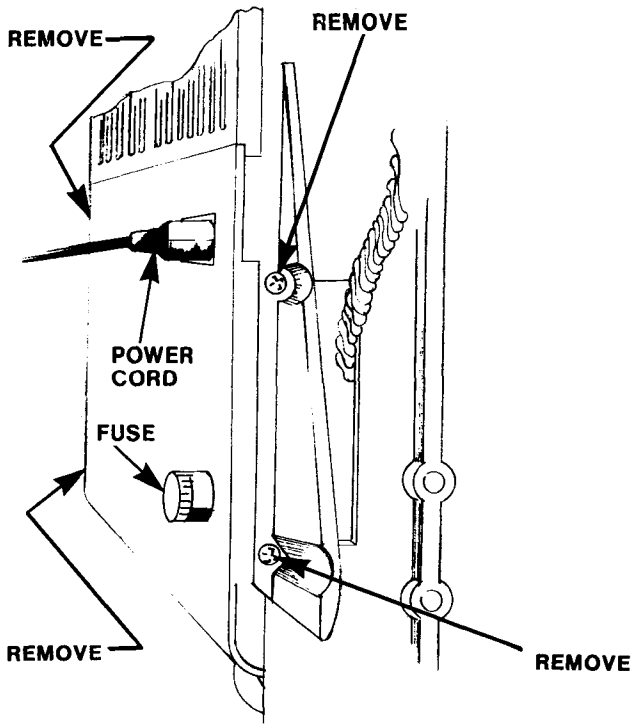


FIGURE 7-14
POWER SUPPLY REMOVAL

7.8 CRT COVER REMOVAL

1. To remove the top cover of the CRT, remove the two screws (shown in Figure 7-15) in the back of the monitor.

2. Slide the cover back and then lift off.

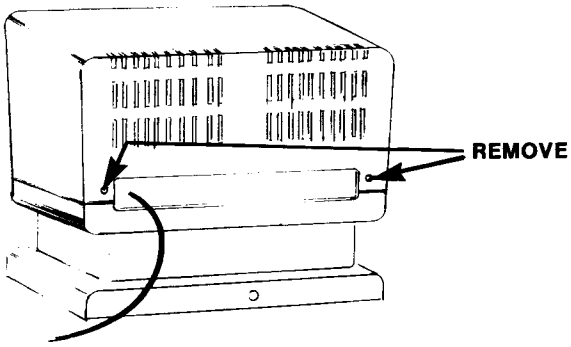


FIGURE 7-15
CRT COVER REMOVAL

7.9 CARRIAGE REMOVAL

1. Remove side covers as specified in paragraph 7.1.

2. Remove the printer from stand as specified in paragraph 7.2.

3. Loosen and remove carriage cords.

4. Remove carriage-rods hold-downs by removing the screws that hold them to the side frame (see Figure 7-16).

5. Remove the flex cable by removing the two screws on the end of the cable that mounts to the carriage (see Figure 7-17). Also remove tie down.

NOTE

The above step will not be performed if a new carriage comes with a cable.

6. Slide the carriage off the rods.

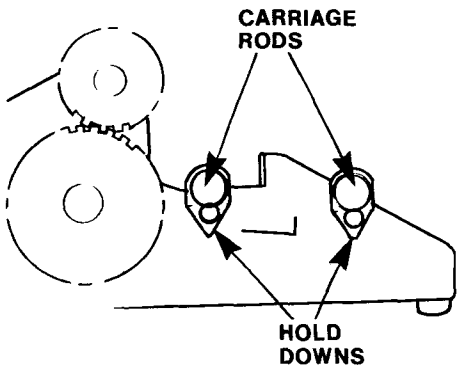


FIGURE 7-16
CARIAGE RODS HOLD DOWNS

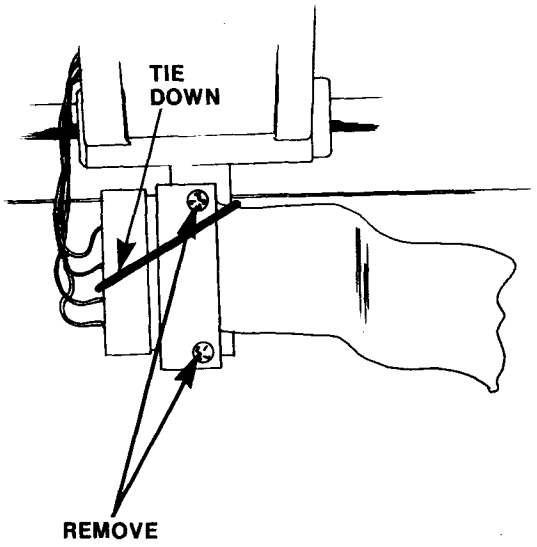


FIGURE 7-17
CARRIAGE FLEXIBLE CABLE

7.10 CORD REPLACEMENT

1. Remove the side covers of the print stand as described in paragraph 7.1.

2. Remove printer as described in paragraph 7.2.

3. Loosen the cord tension by removing screw, (1) of Figure 7-18.

4. Put the ball end of the cord in the bottom hole of the carriage hub, see (2).

NOTE

In handling cords, a spring hook will be helpful.

5. Now with the loop end of the cord, feed the cord around the right-hand pulley, see (3).

6. Take the loop end of the cord and push the loop end through the hole in the right-hand side frame, and put on the holding pin to fasten the end, see (4).

7. Now, with the spring hook, loop the cord around the top groove of carriage pulley with the carriage about two inches from the left-side frame, see (5).

8. Turn the hub clockwise a couple of times to get a couple loops on the hub. Hold the hub tight and pull the cord out at the point between the hub and the pulley, to cause the carriage to slide to the right side of the printer to within an inch or so of the right side. (This will give you room to wind up the rest of cord without interference from the carriage, see (6).

9. Take the second cord and put the ball end of the cord in the top hole of the hub. Wrap the cord clockwise around the hub two full turn and have it come off the front of the hub, see (7).

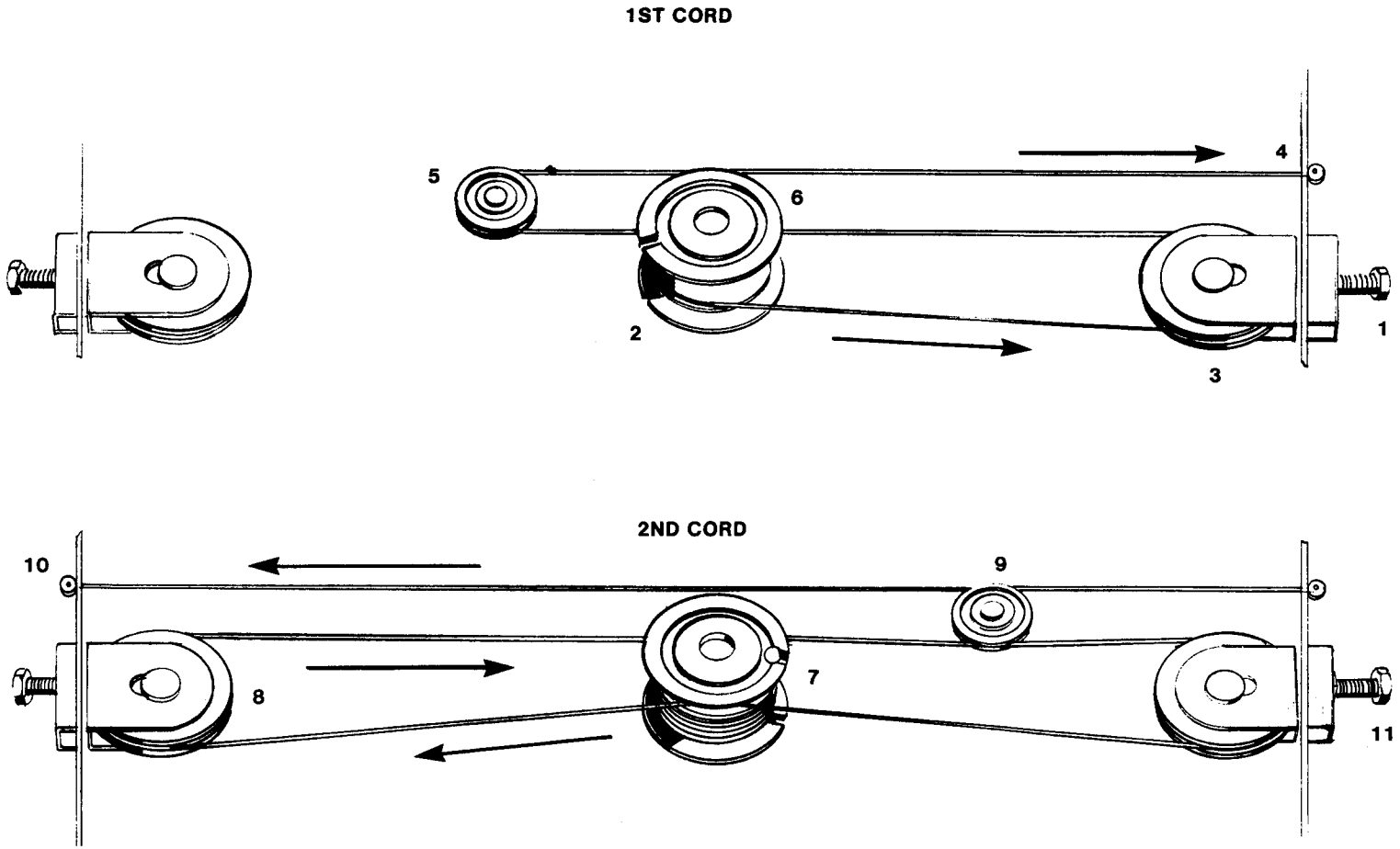


FIGURE 7-18 CORD REPLACEMENT

10. Take the loop end of the cord and feed it around the left pulley, see (8).

11. Loop the cord around the bottom groove of the carriage pulley with a spring hook, see (9).

12. Stick the loop end of the cord through the left-side frame and put the holding pin in, see (10).

13. Now tighten the cord tension.

14. Replace printer.

15. Replace side covers.

7.11 PHOTO SENSOR

All photo sensors (5) are easily removed by unscrewing them from the printer, and removing their leads from the connectors. Right and left carriage sensor leads may be cut under the printer base and replacement soldered in place.

7.12 PAPER FEED TRAY REMOVAL

The paper-feed tray is removed from the printer by loosening the two thumb screws in the back of the tray.

7.13 PLATEN ASSEMBLY REMOVAL

The platen assembly can be removed by releasing the latches on each side then lifting the platen up and out.

7.14 SYSTEM KEYBOARD REMOVAL

The CRT keyboard is removed by removing the three screws just below the function keys under the plastic logo strip. (This allows one to remove the top cover of the keyboard.) Then remove the four keyboard-mounting screws and the connector that plugs into the keyboard.

7.15 CARD GUIDE REMOVAL

The card guide is removed by removing the two screws on the mounting bracket.

7.16 HAMMER REMOVAL

CAUTION

Be careful of the hammer because it is spring loaded and can pop out unexpectedly.

To remove the hammer, remove one of the two hammer bracket mounting screws; loosen the other, and tip up one end of the bracket. Once this is done, the hammer can be slid out of the housing.

7.17 PRINT WHEEL REMOVAL

Print wheel removal is done by tilting the ribbon platform back. This will cause the ribbon to lift automatically. Now pull on the print wheel hub. It will lift off easily.

7.18 CRT PCA REMOVAL

1. Remove CRT cover as specified in paragraph 7.8.
2. Remove PCA by just pulling it out of its socket.

CHAPTER 8

ILLUSTRATED PARTS BREAKDOWN

The following table, in conjunction with Figures No. 8-1 through 8-29, provides a photographic identification of most spares to be stocked at the various maintenance levels. The identification callouts (ITEM NO.) provide transition between figures and table; the decimal composition of each callout indicates the next higher assembly of the respective item. Should an OEM equivalent (where applicable) of a given part number be required, reference may be made to Appendix L, Recommended Spares List, for translation between the respective numbers.

ITEM NO.	PART NO.	FIGURE	DESCRIPTION
0	177-9450	8-1	Wang Writer Model 5503
1.0		8-1, 2	Printer Unit
1.1	279-9000-35	8-2	Switch Assembly, Cover Open
1.2	449-0423	8-2	Feed Tray
1.3	299-9000-10	8-3	Printer Assembly
1.3.1	279-9000-22	8-4	Print Head Assembly
1.3.1.1	358-0398	8-5	Printer Hammer
1.3.1.2	375-2110-4	8-6	End-of-Ribbon Sensor
1.3.2	279-9000-20	8-6	Platen Assembly
1.3.3	220-3139	8-7	Print Head Flex Cable Assembly
1.3.4	279-9000-26	8-7	Carriage Drive Motor Assembly
1.3.5	279-9000-27	8-8	Paper Drive Motor Assembly
1.3.6	420-1033	8-9	Carriage Drive Cable
1.4	210-7776	8-10	Printer PCA
1.4.1	340-0017	8-10	7-Segment Display
1.4.2	360-1155	8-10	2-Amp Fuse (F2, F3)
1.4.3	360-1156	8-10	4-Amp Fuse (F1)
1.5	210-7777	8-11, 12	CPU PCA
1.5.1		8-12	System Option Switches
1.6	210-7775	8-13	Memory PCA
1.6.1	378-3035	8-13	E-PROM 2908-0 (CRT Char Gen)
1.6.2	377-0345-T	8-13	16K X 1-Bit Dynamic RAM
1.6.3	377-0341-L	8-13	1024 X 4-Bit Static RAM

ITEM NO.	PART NO.	FIGURE	DESCRIPTION
1.7	360-1016-33	8-14	Switch Panel Assembly
1.8	456-1236	8-15	Card Guide
1.9	278-4022	8-16, 17	Disk Drive Assembly
1.9.1	220-3131	8-16	Floppy Logic Cable Assembly
1.9.2	726-8070	8-16,18,19	Disk Drive PCA
1.9.3	370-0026	8-17	Red LED
1.9.4	726-8069	8-17	Disk Drive Belt
1.10	279-9000-32	8-20	Power Supply
1.10.1	360-1016-SB 360-1031-SB	8-20	1 1/2 Amp at 230V or 3 Amp at 115V
1.10.2	323-0010	8-20	6-Digit Printer Char Counter, 12V
1.10.3	279-9000-34	8-21, 22	Power Supply Regulator & Heat Sink Assembly
1.10.4	400-1012	8-21	Muffin Fan
1.10.5	360-1154	8-21, 22	Fuse, 18V Reg., 125V/1A, Pico
2.0	279-9000-70	8-1, 23	Monitor Module
2.1	210-7456	8-23, 24	CRT Electronics PCA
2.2	270-0689	8-25	12-inch Monitor & Frame Assembly
2.2.1	220-0262	8-25	CRT Cable Assembly
2.2.2	340-0108	8-25, 26	12-Inch CRT Tube
3.0	279-9000-90	8-1, 27	Keyboard Module
3.1	220-1505	8-27	Keyboard Cable Assembly
3.2	271-1222 (Wang) or 725-2635 (Keytronic)	8-28	Keyboard Assmelby
3.3	449-0372	8-29	Keyboard Base
3.3.1	279-9000-91	8-29	Speaker Assembly

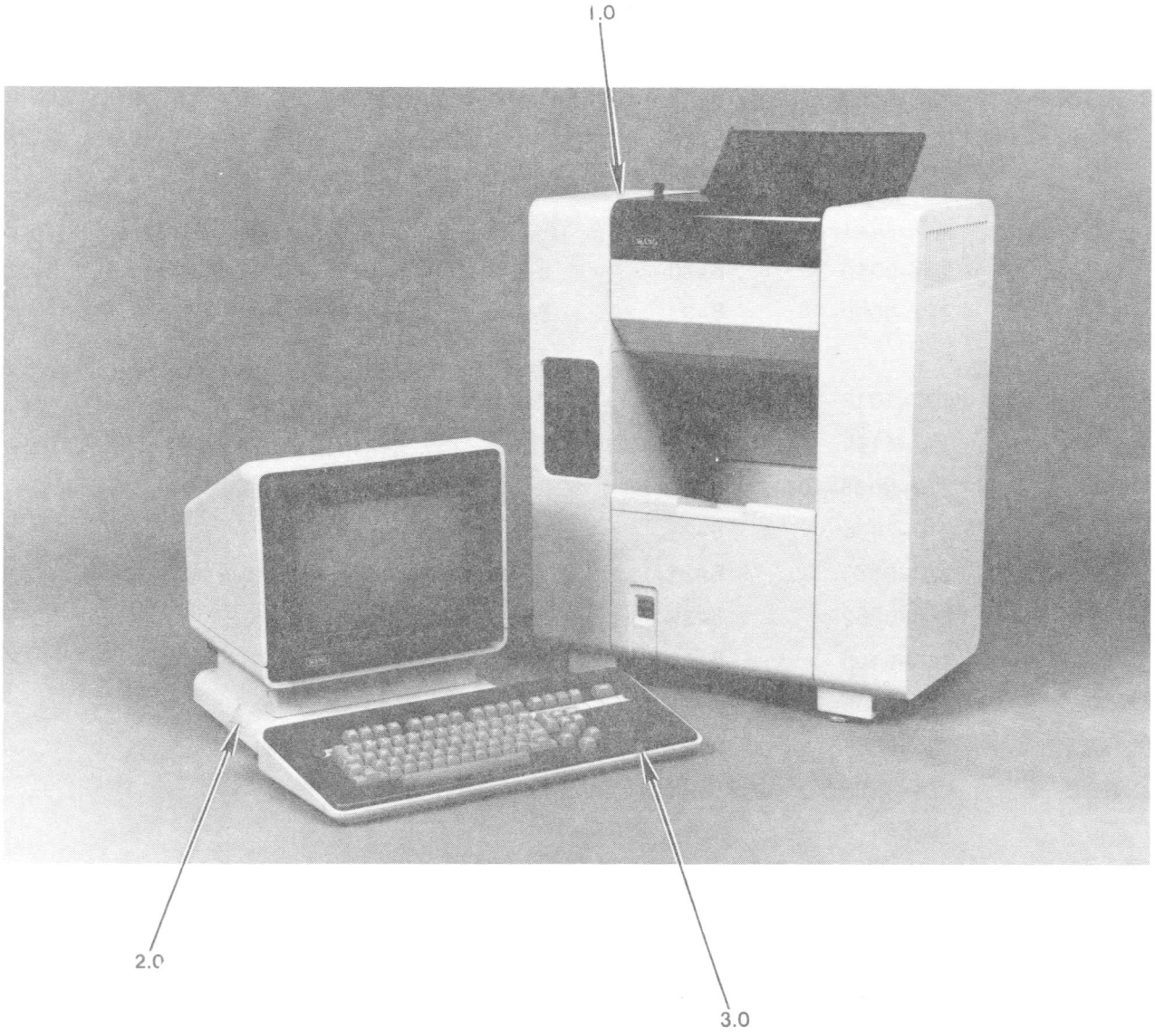


FIGURE 8-1 WANGWRITER MODEL 5503

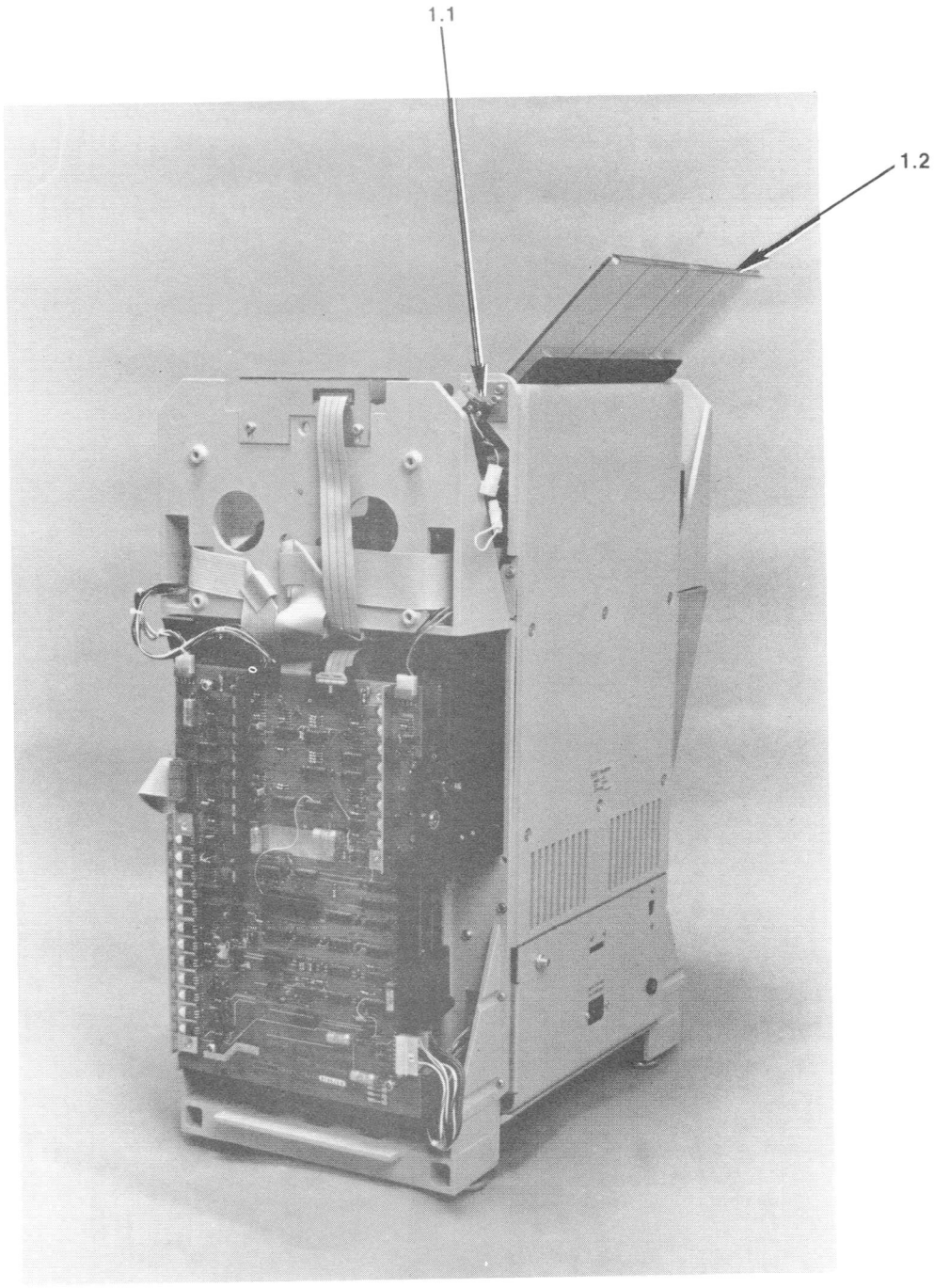


FIGURE 8-2 PRINTER UNIT (ITEM 1.0), COVERS REMOVED

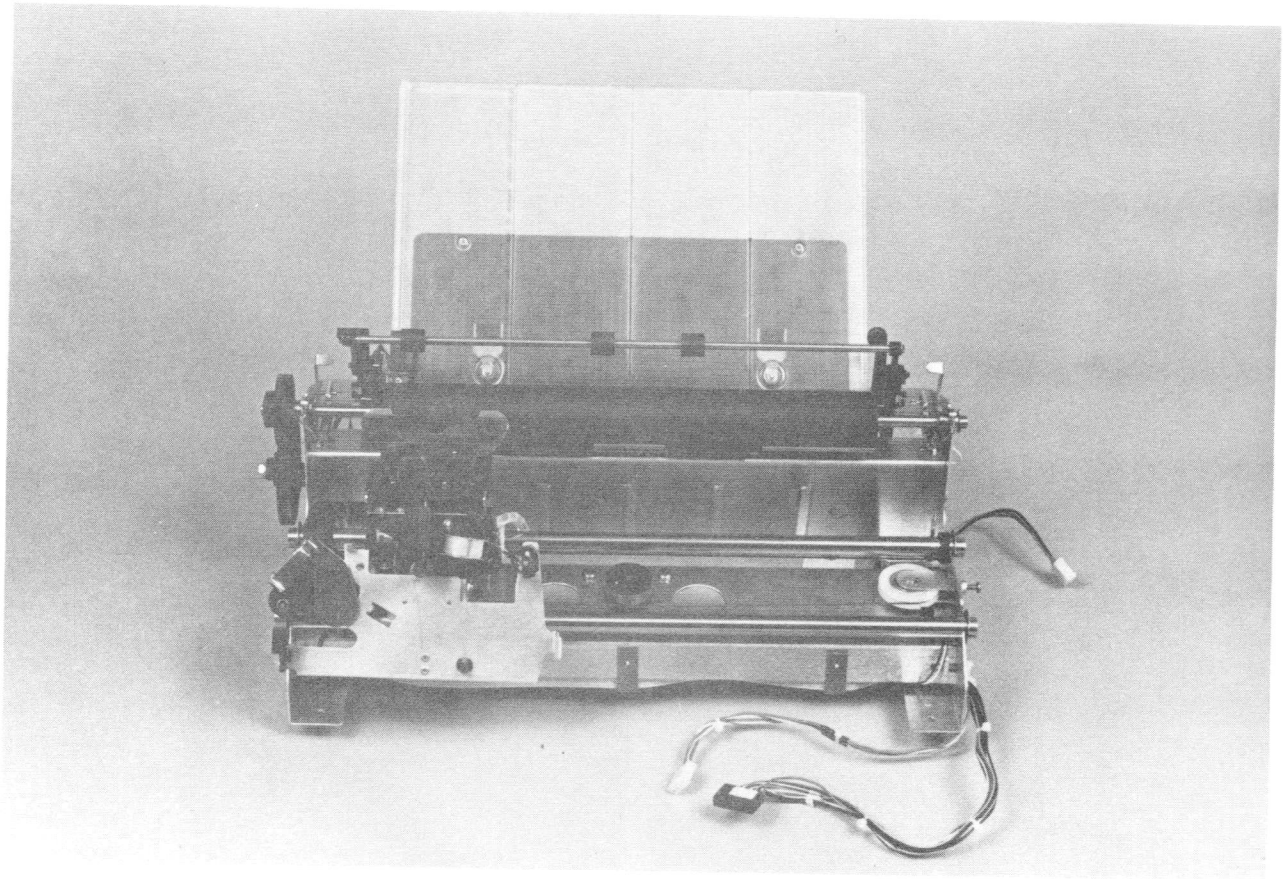


FIGURE 8-3 PRINTER ASSEMBLY (ITEM 1.3)

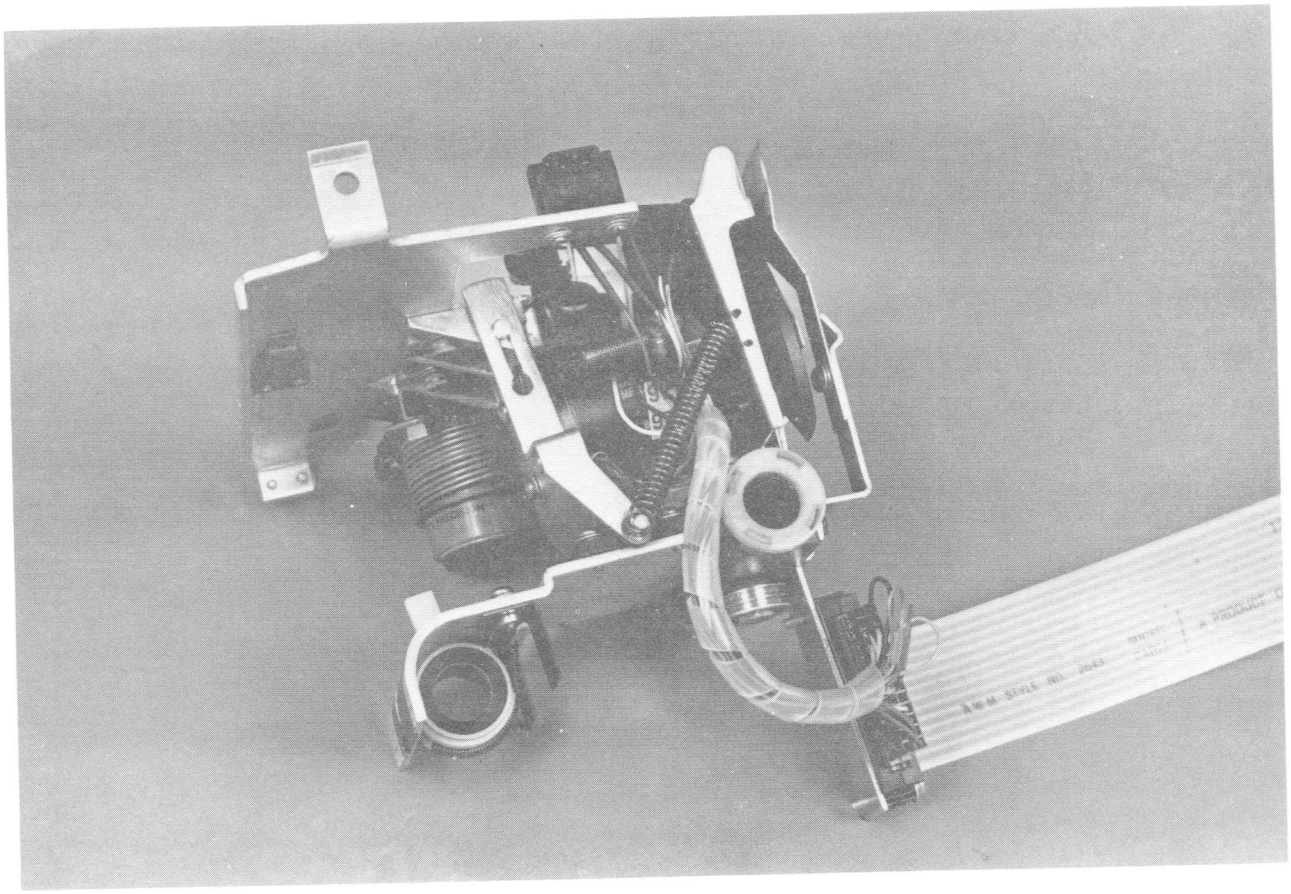


FIGURE 8-4 PRINT HEAD ASSEMBLY (ITEM 1.3.1)

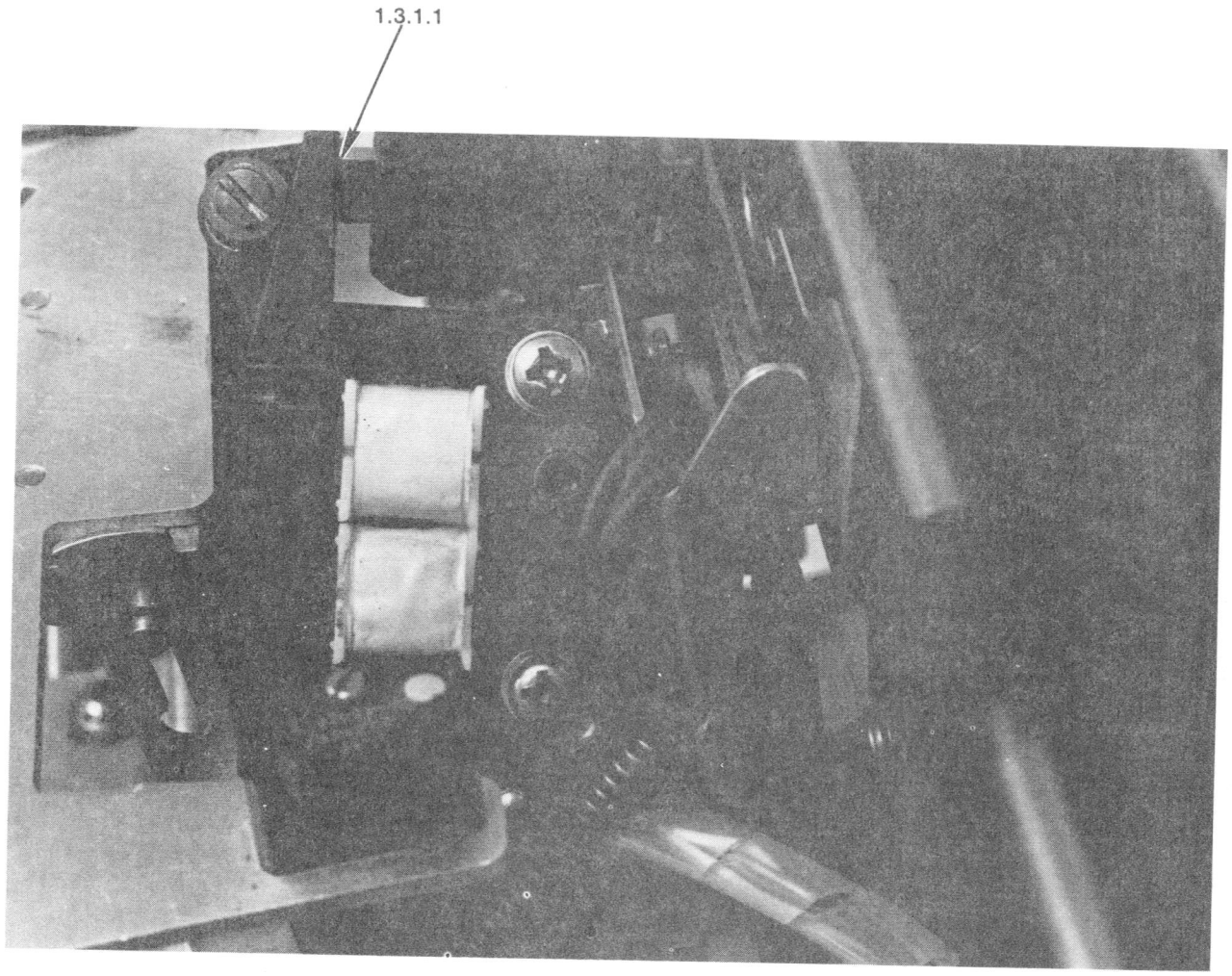


FIGURE 8-5 PRINTER HAMMER (ITEM 1.3.1.1)

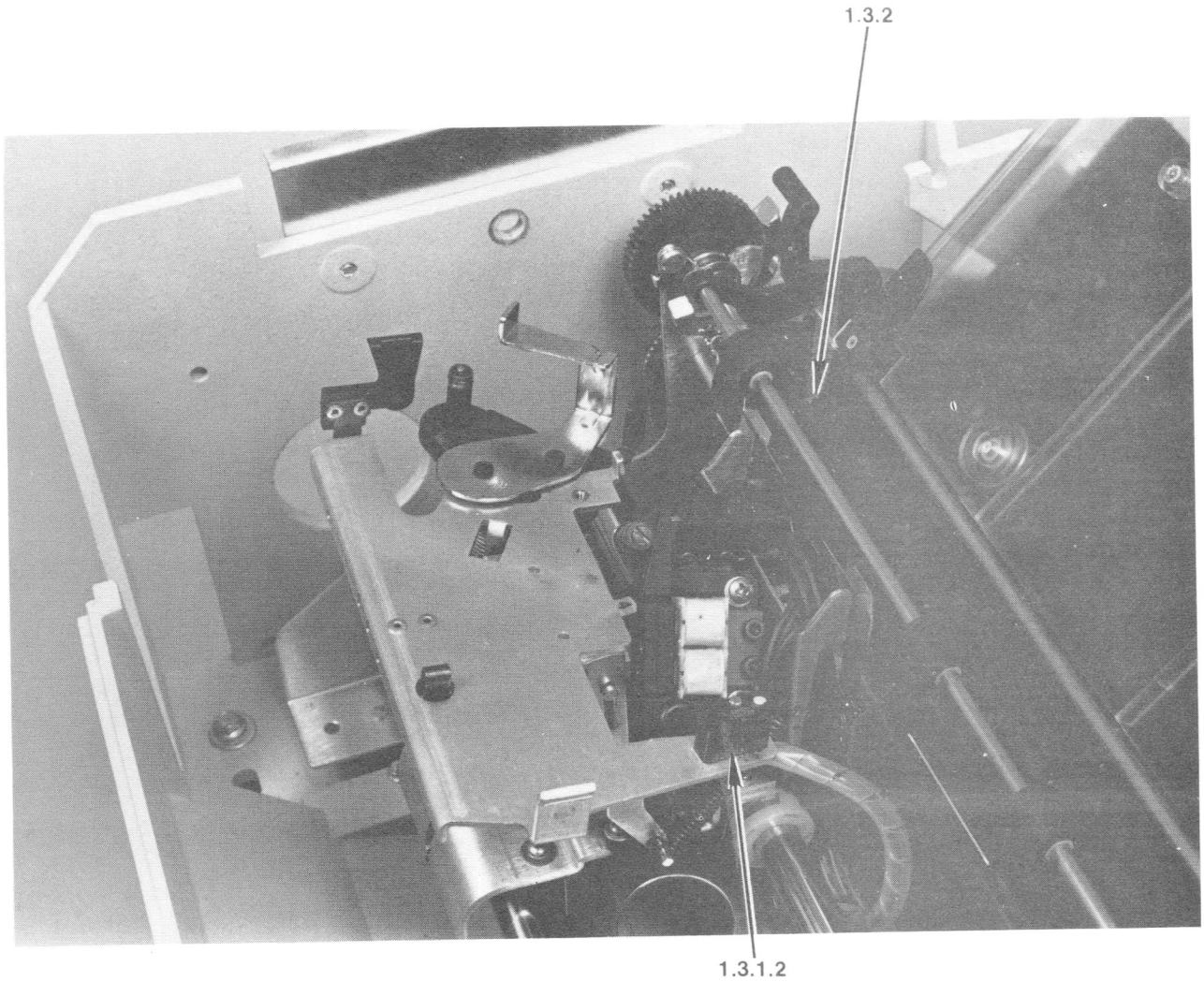


FIGURE 8-6 END-OF-RIBBON SENSOR (ITEM 1.3.1.2) AND PLATEN ASSEMBLY (ITEM 1.3.2)

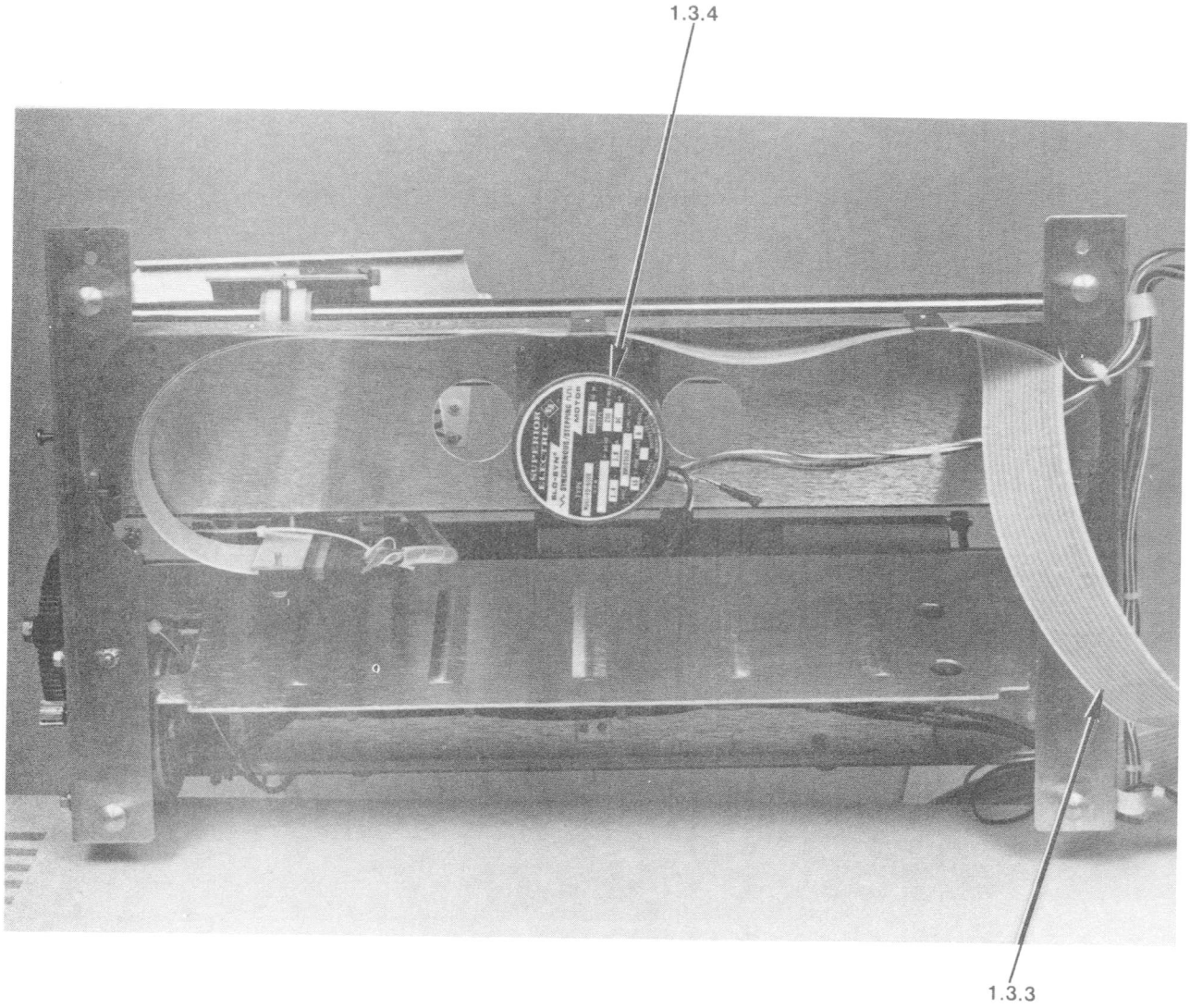


FIGURE 8-7 PRINT HEAD FLEX ASSEMBLY (ITEM 1.3.3)
AND CARRIAGE DRIVE MOTOR ASSEMBLY (ITEM 1.3.4)

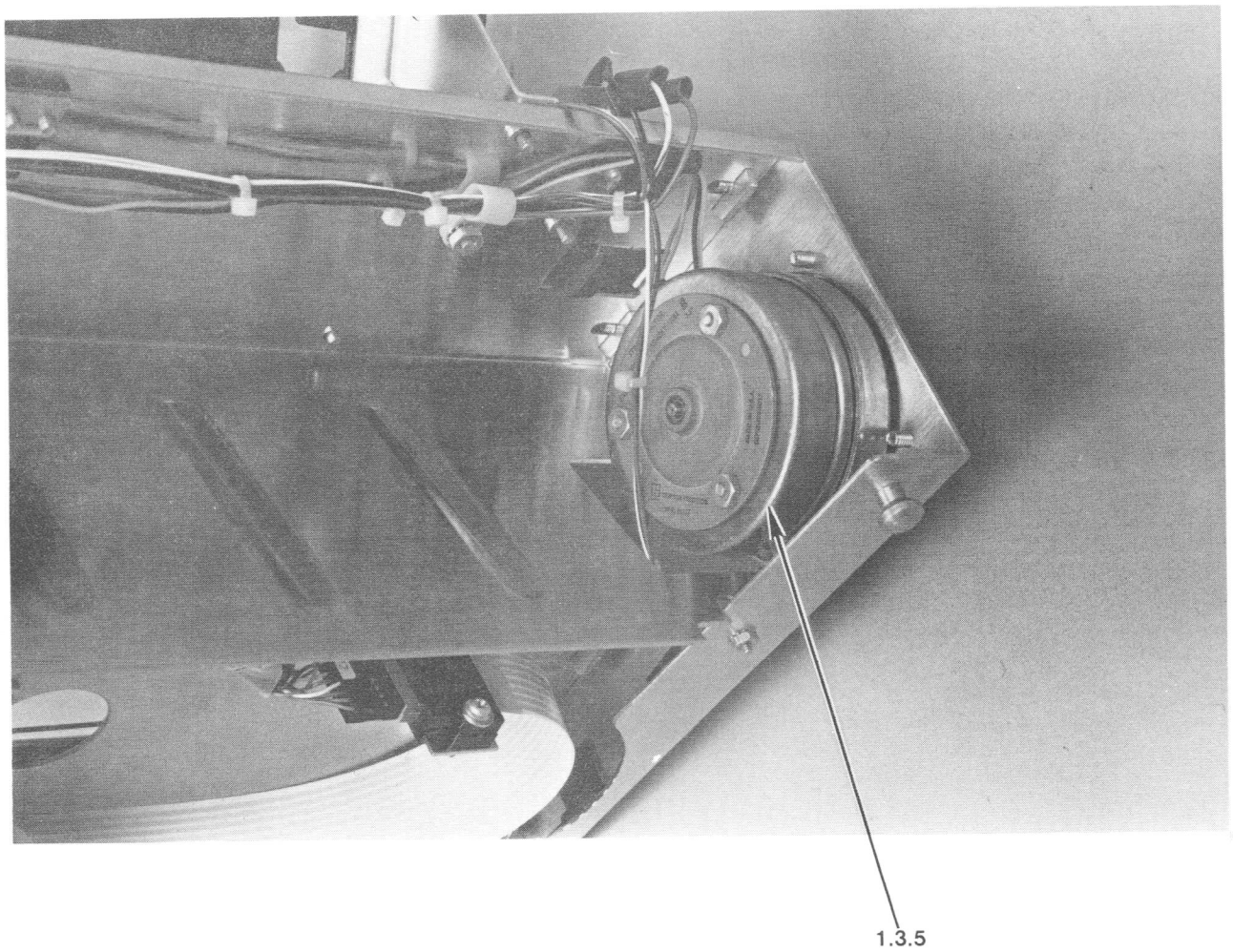


FIGURE 8-8 PAPER-DRIVE MOTOR ASSEMBLY (ITEM 1.3.5)

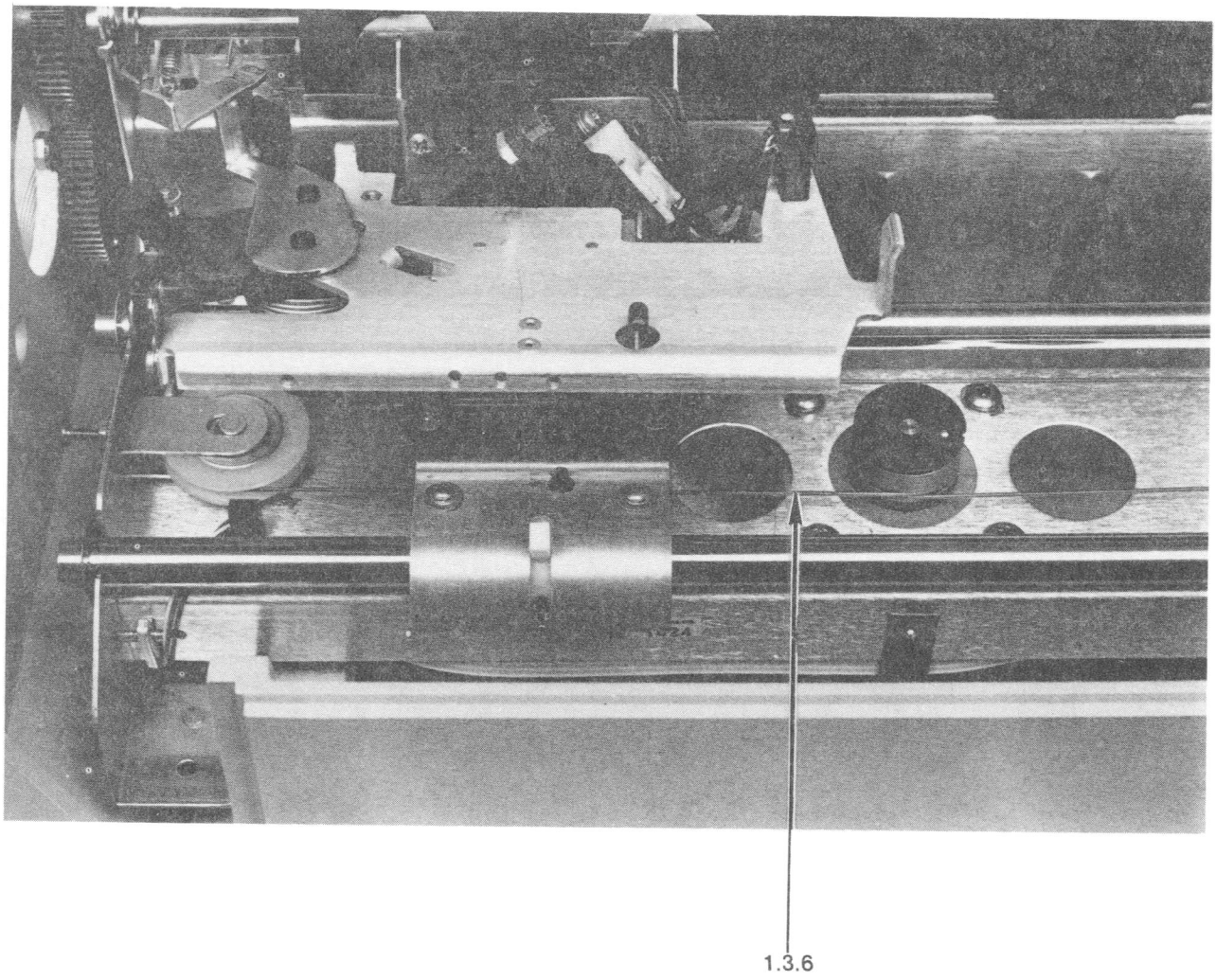


FIGURE 8-9 CARRIAGE DRIVE CABLE (ITEM 1.3.6)

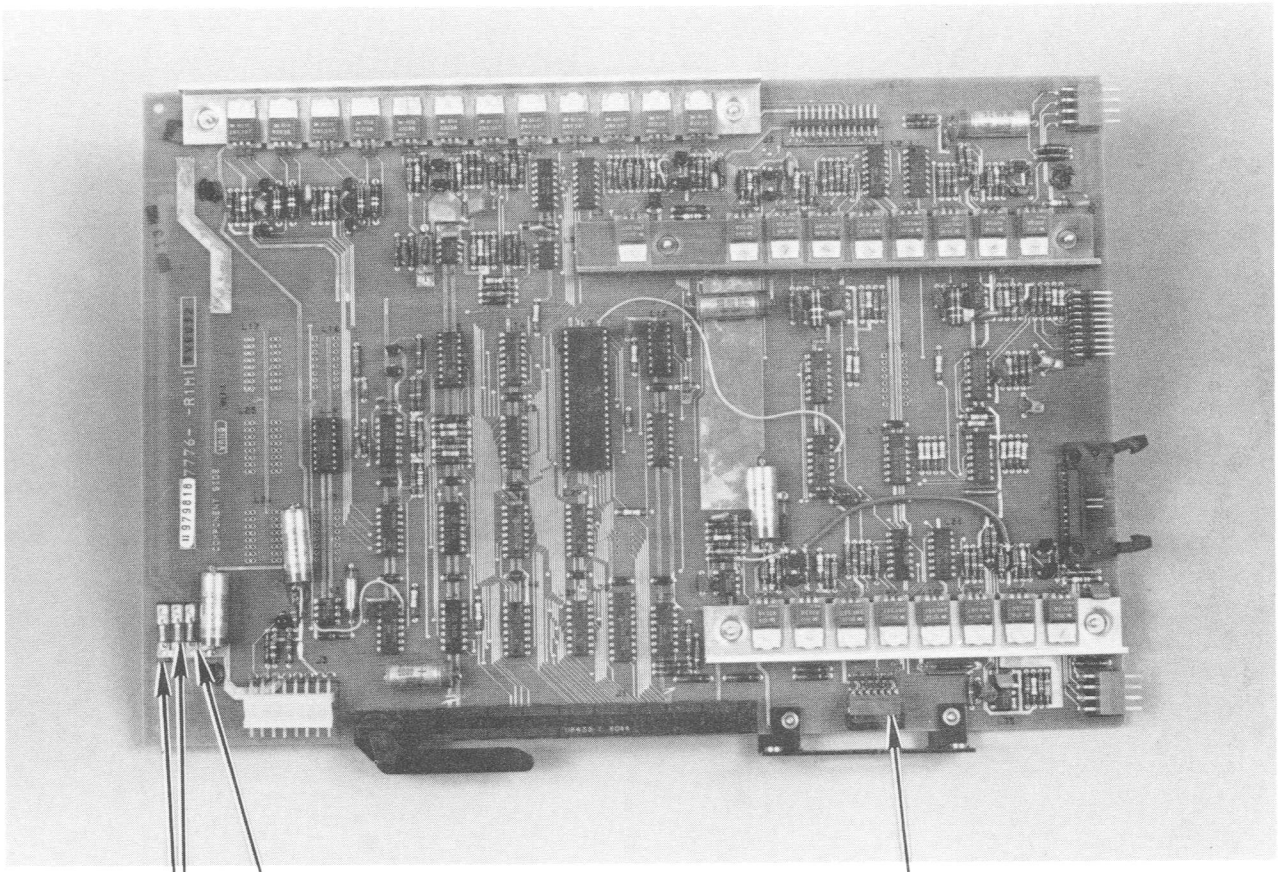


FIGURE 8-10 PRINTER PCA (ITEM 1.4)

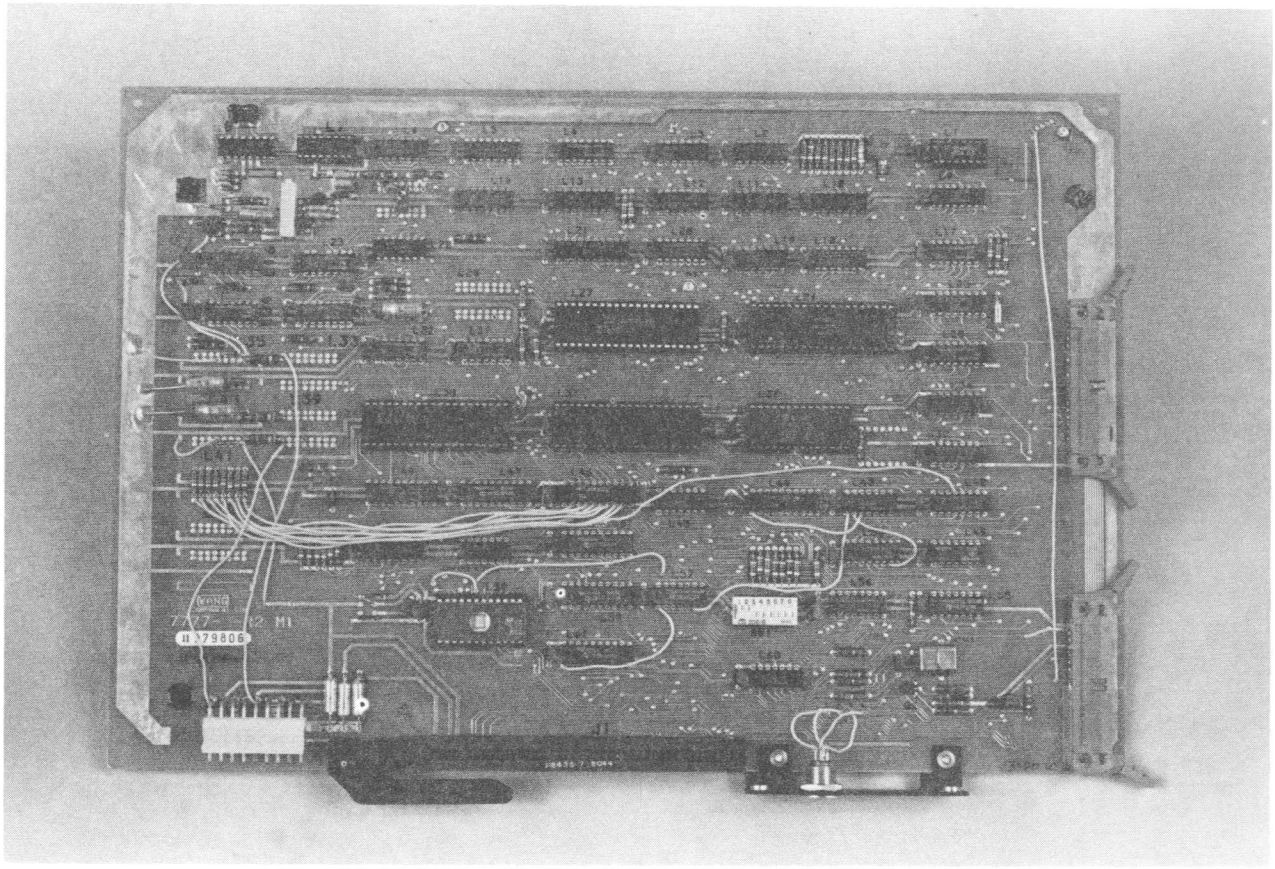


FIGURE 8-11 CPU PCA, COMPONENT VIEW (ITEM 1.5)

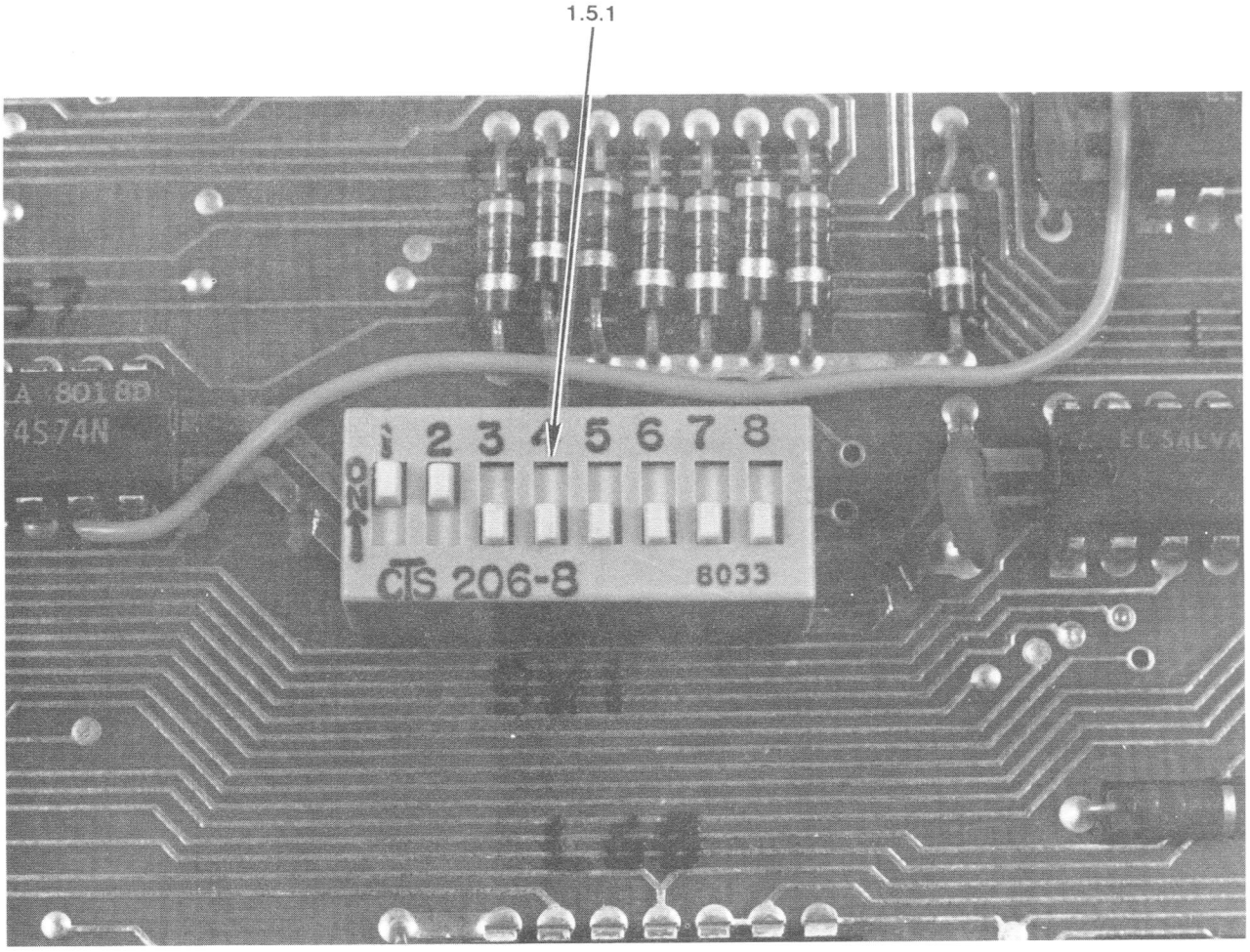


FIGURE 8-12 CPU PCA REVERSE SIDE VIEW (ITEM 1.5)

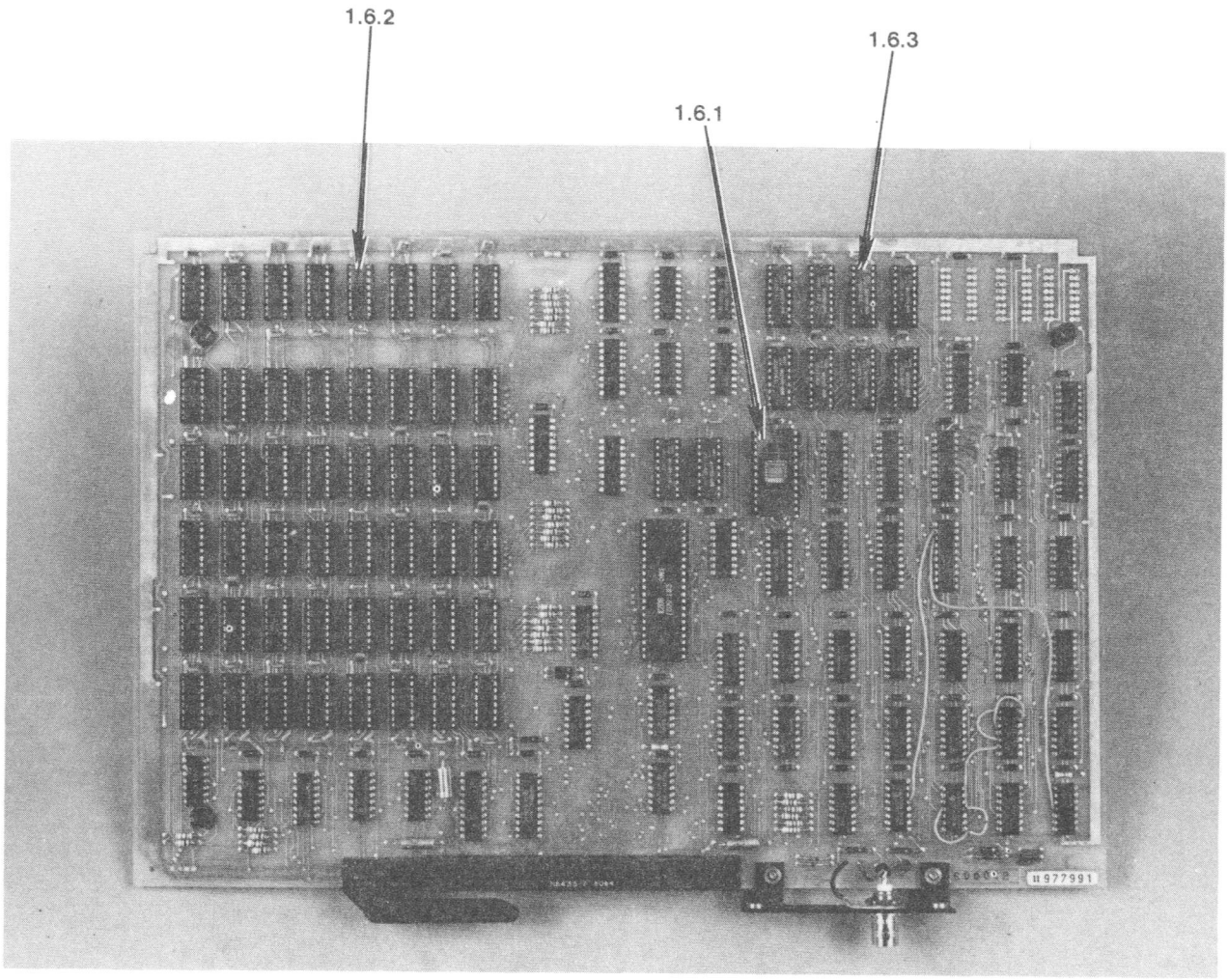


FIGURE 8-13 MEMORY PCA (ITEM 1.6)

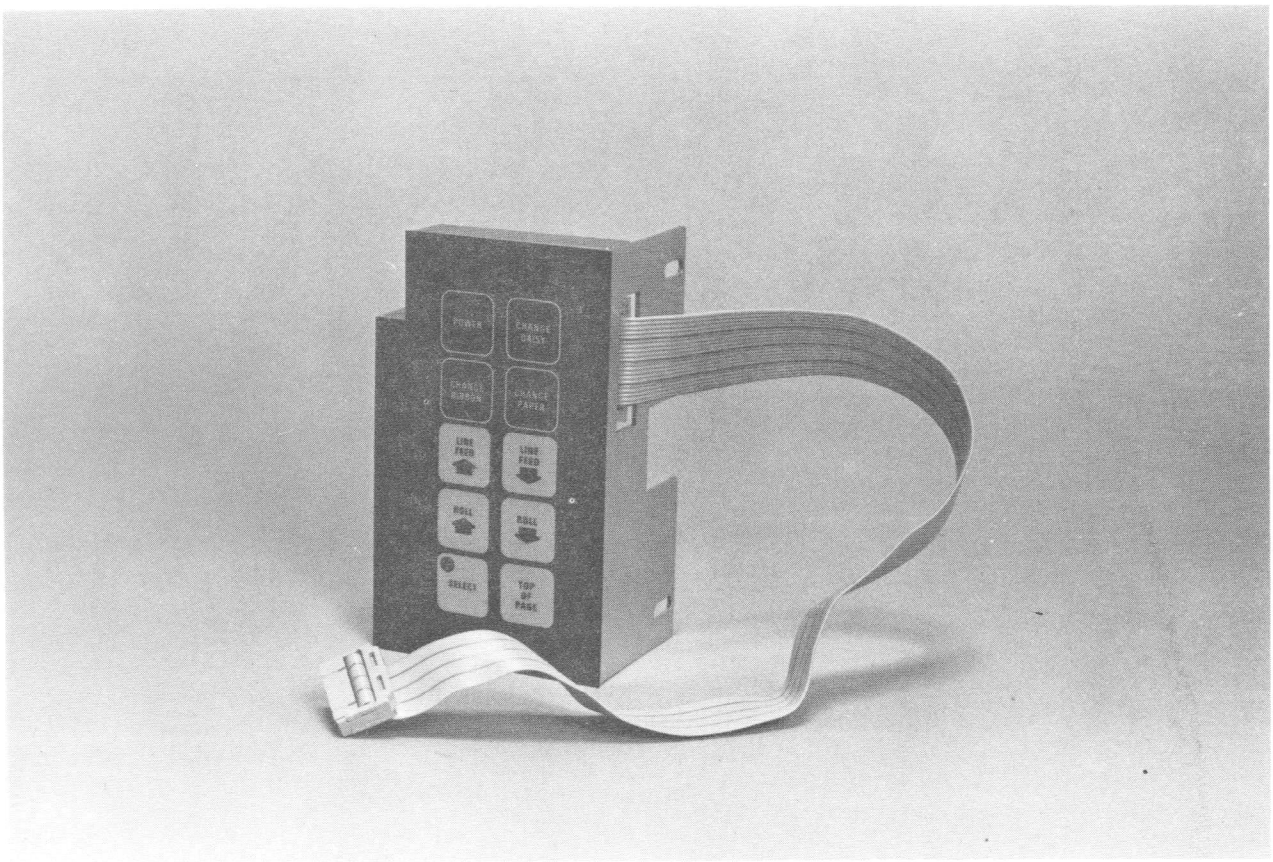


FIGURE 8-14 SWITCH PANEL ASSEMBLY (ITEM 1.7)

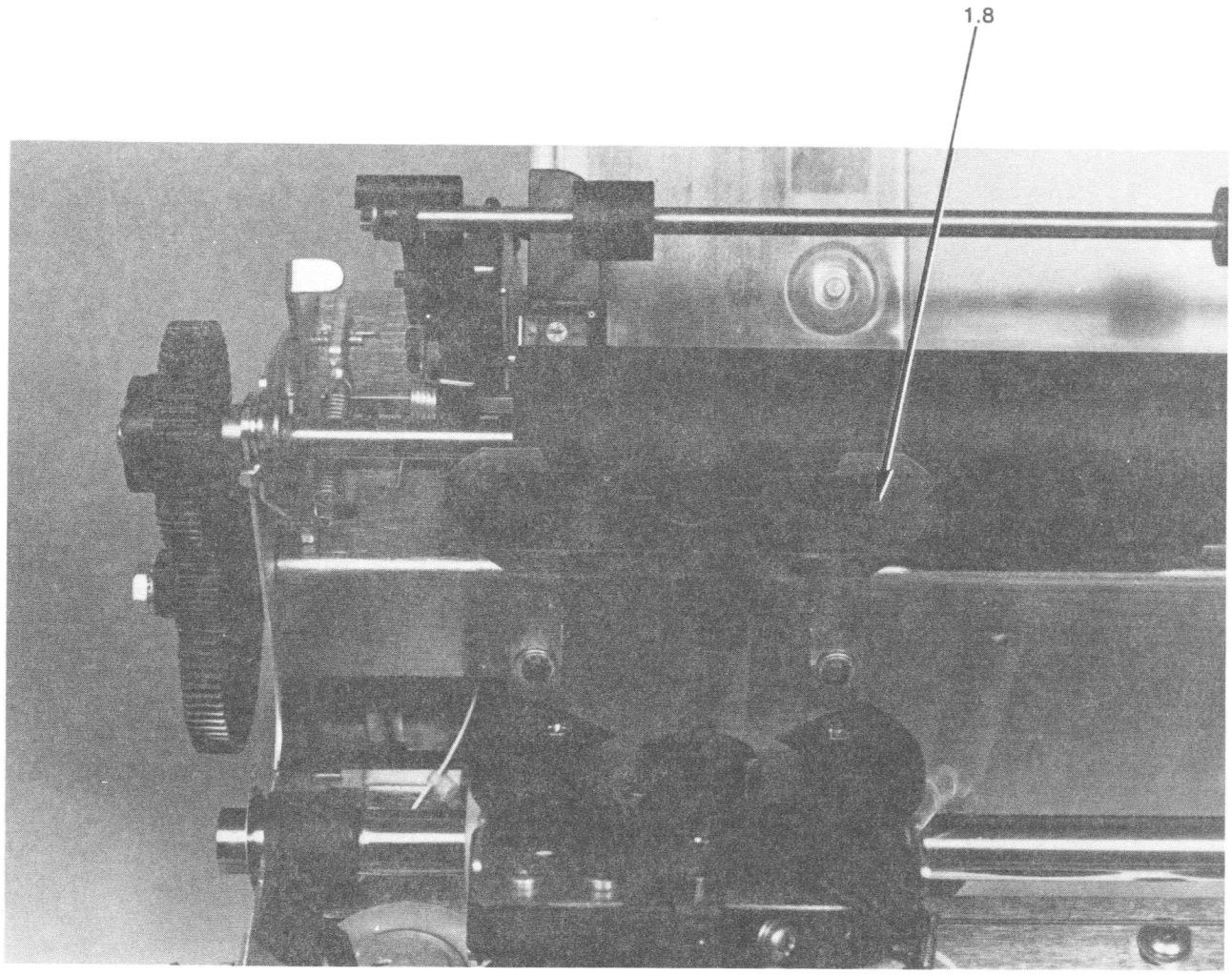


FIGURE 8-15 CARD GUIDE (ITEM 1.8)

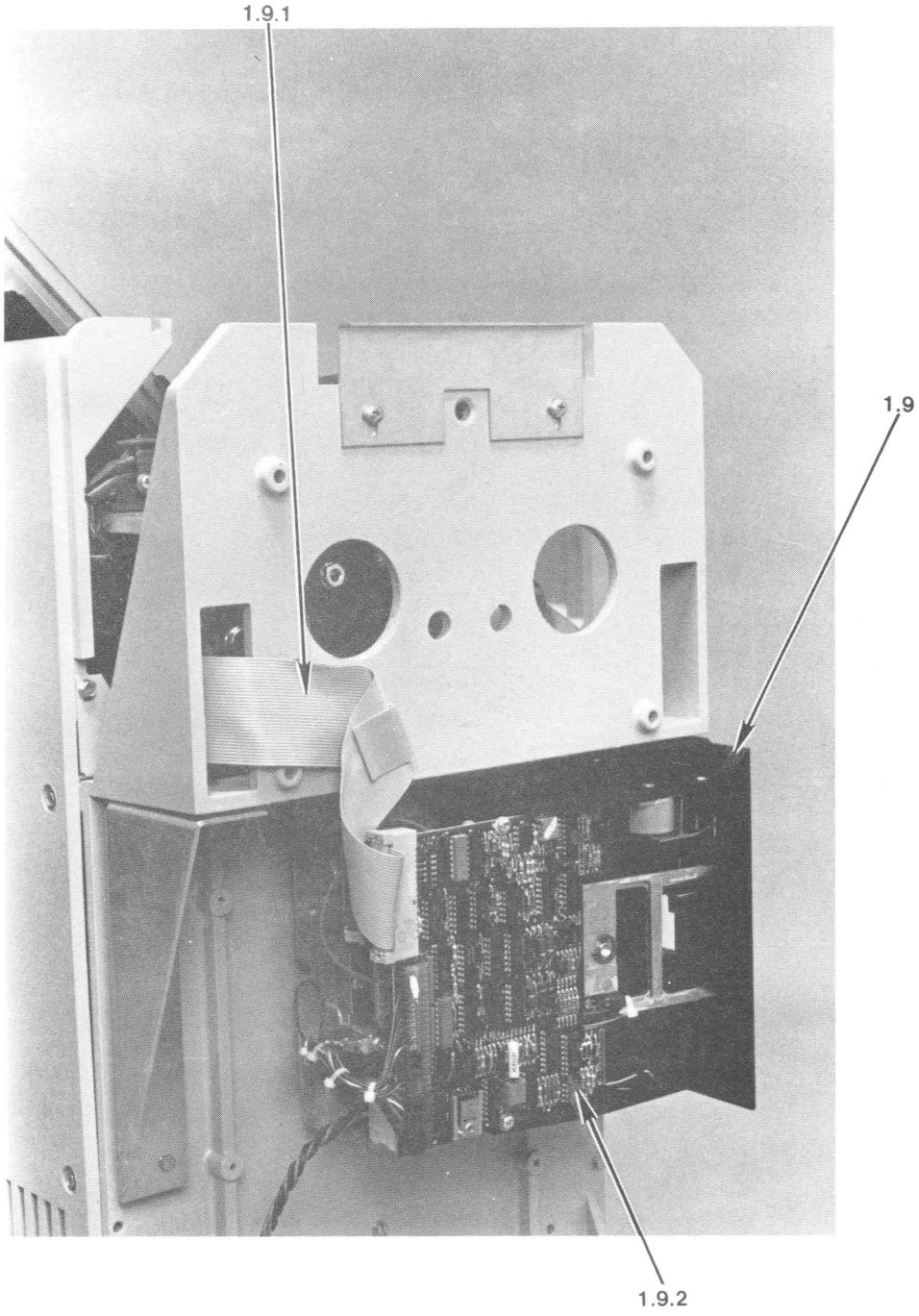


FIGURE 8-16 DISK DRIVE ASSEMBLY (ITEM 1.9)

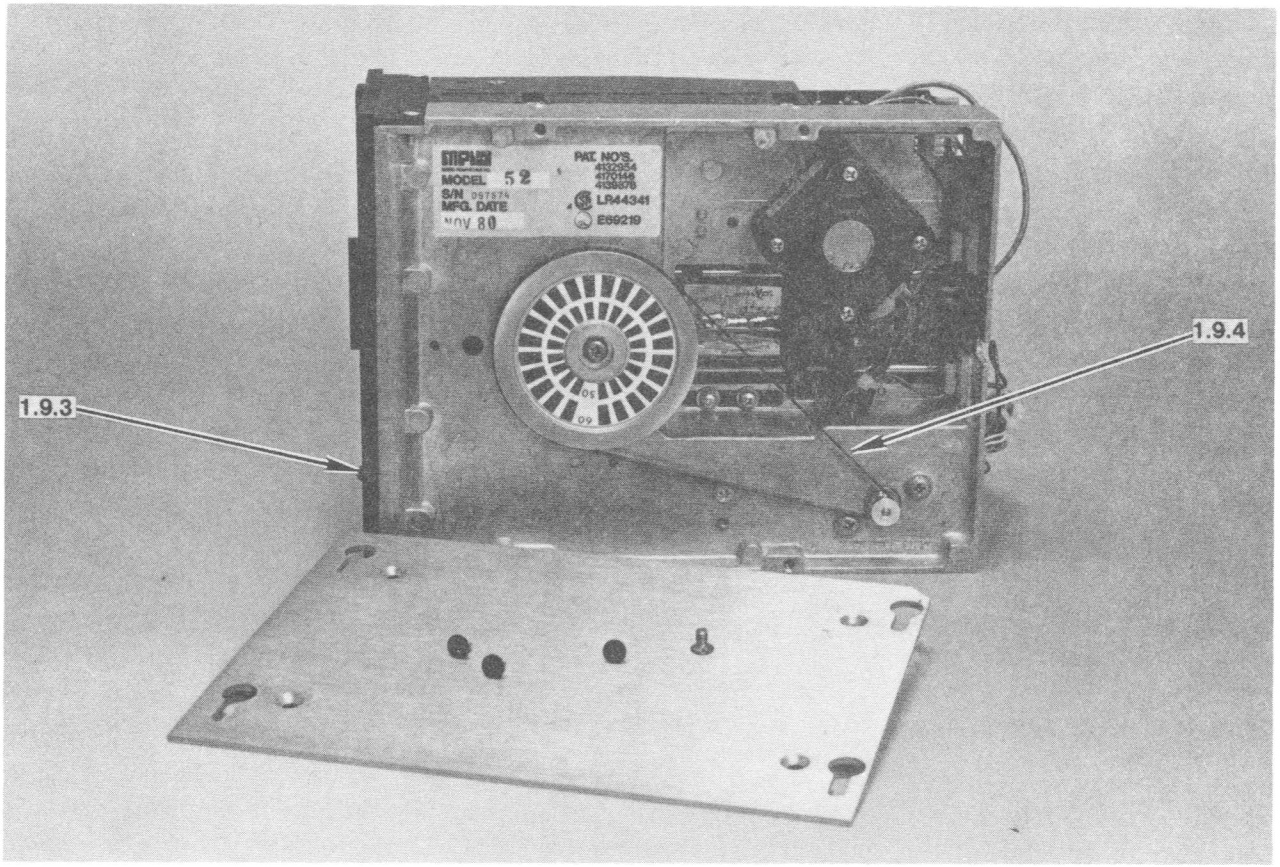


FIGURE 8-17 DISK DRIVE ASSEMBLY (ITEM 1.9) COVER REMOVED

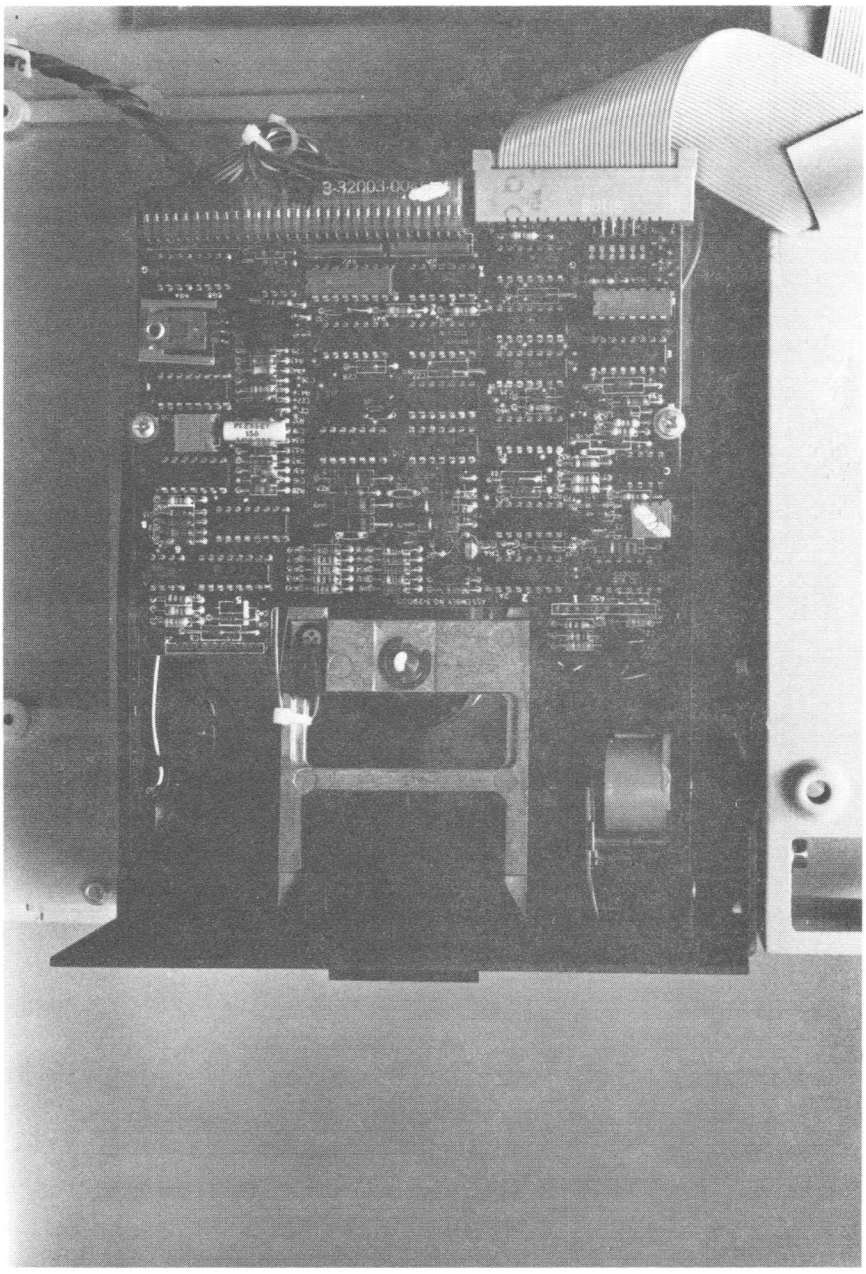


FIGURE 8-18 DISK DRIVE PCA (ITEM 1.9.2), COMPONENT VIEW

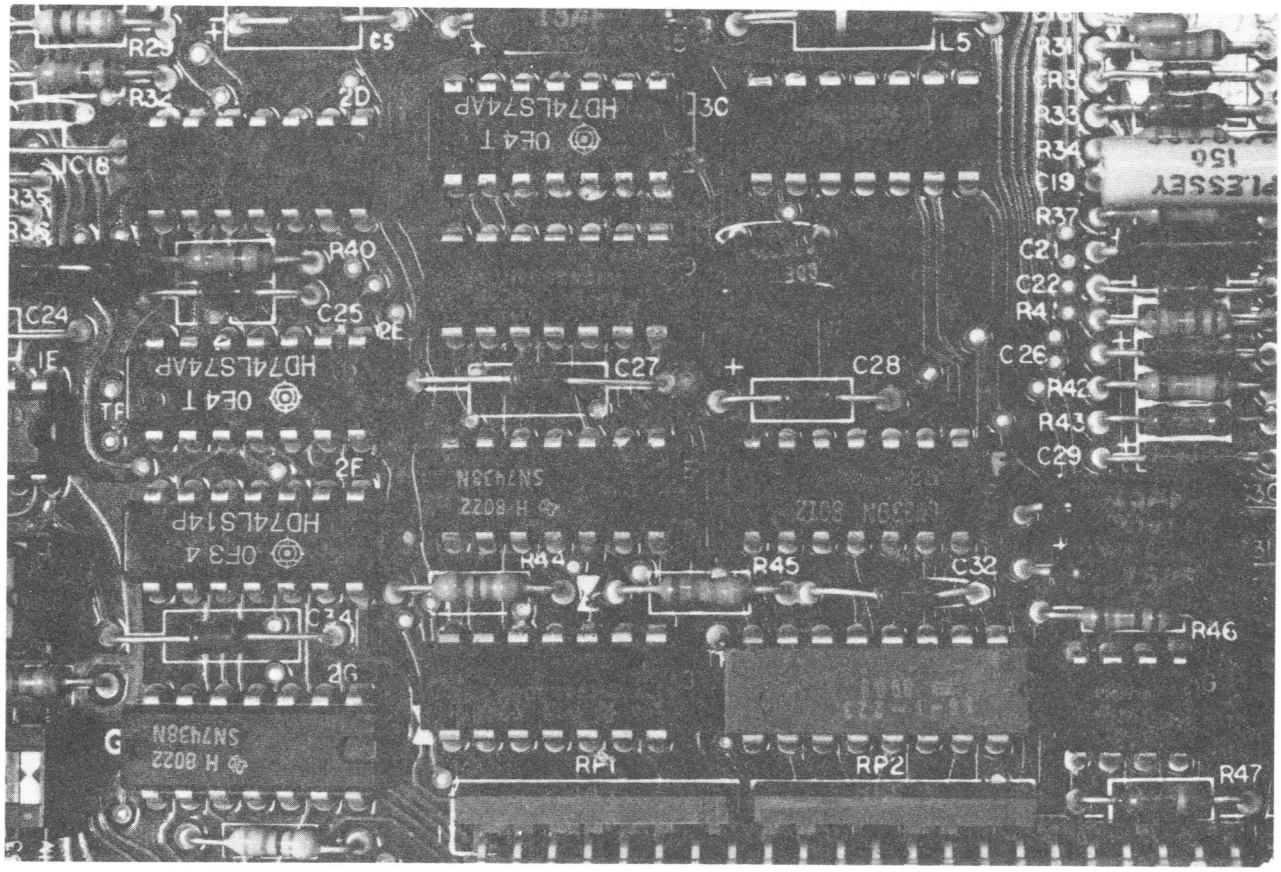


FIGURE 8-19 DISK DRIVE PCA (ITEM 1.9.2). REVERSE SIDE

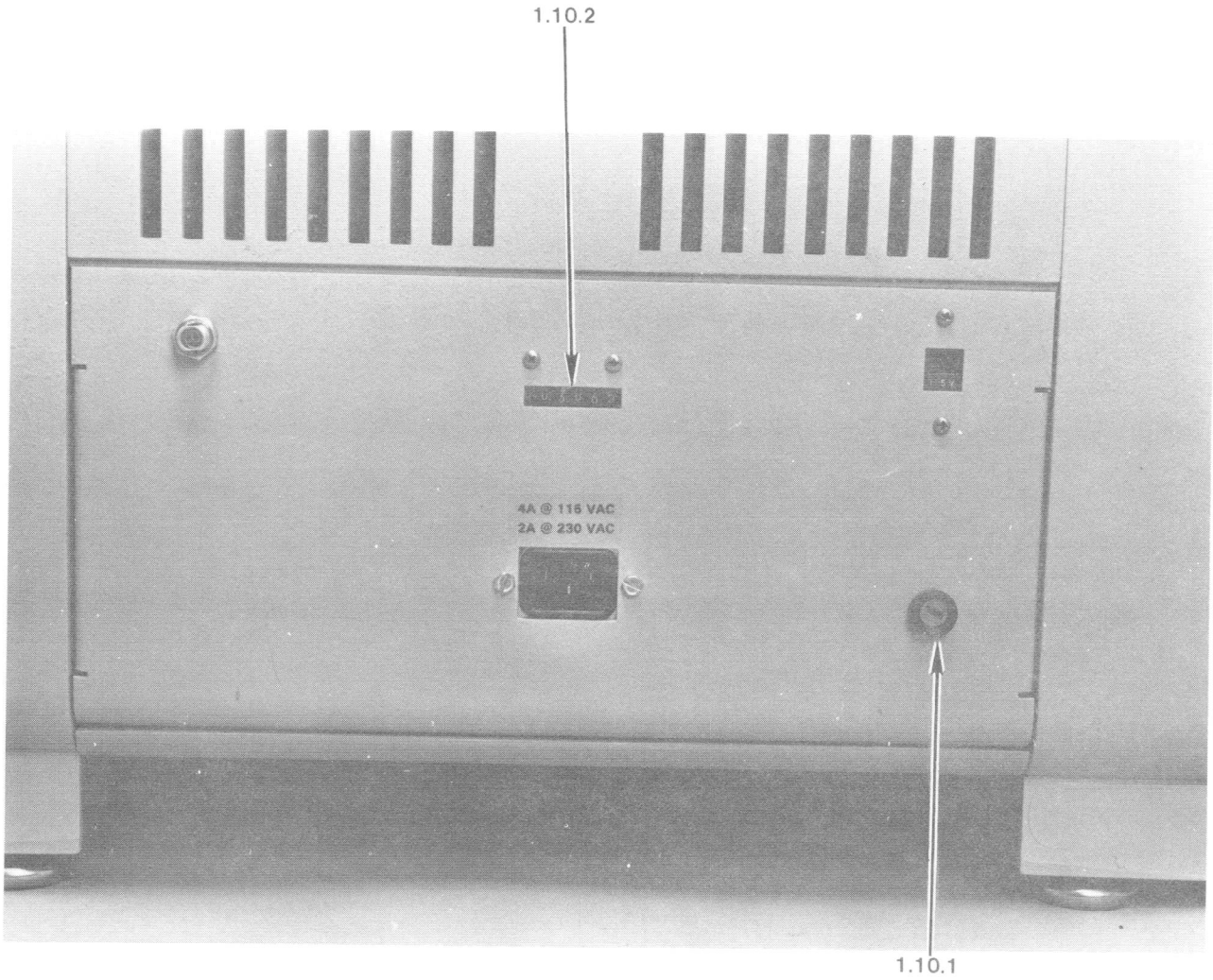


FIGURE 8-20 POWER SUPPLY (ITEM 1.10)

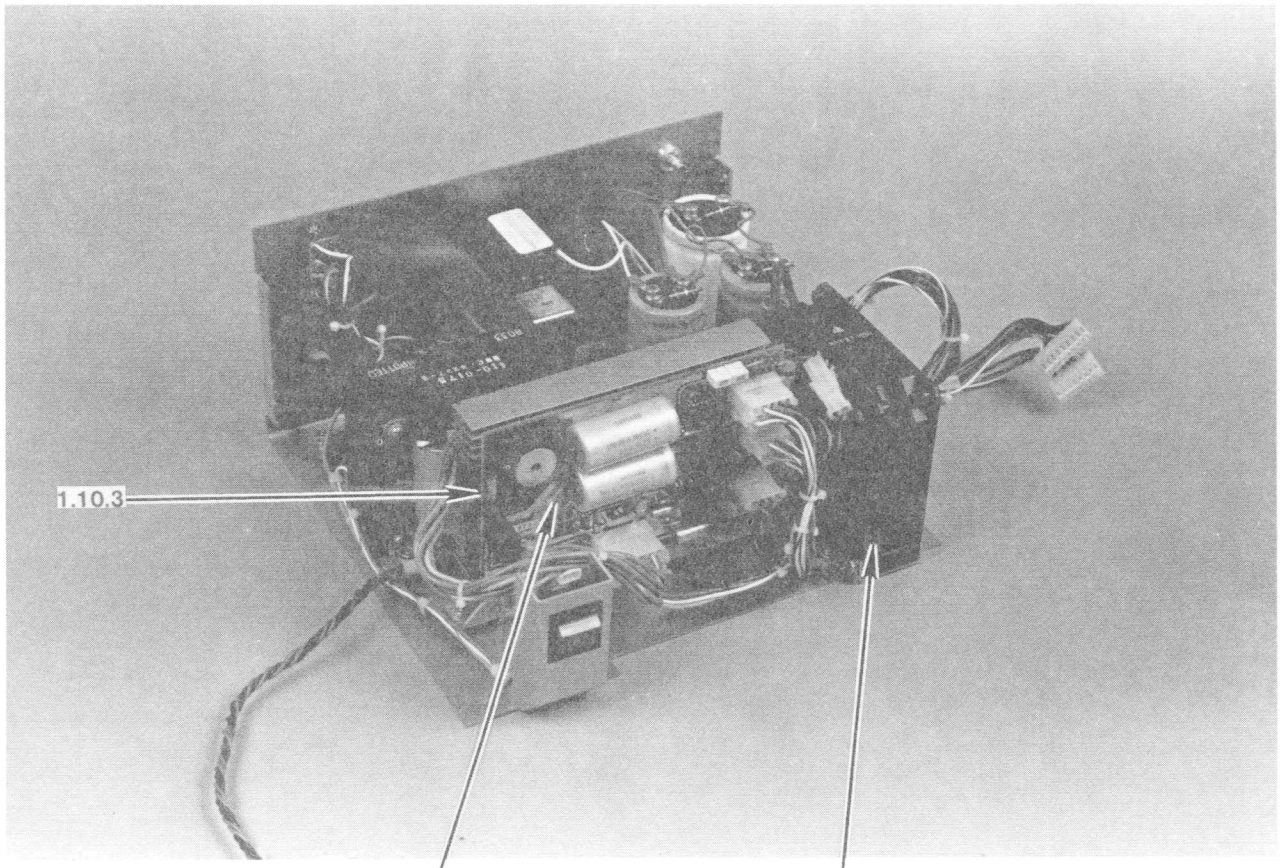


FIGURE 8-21 POWER SUPPLY CHASSIS (ITEM 1.10)

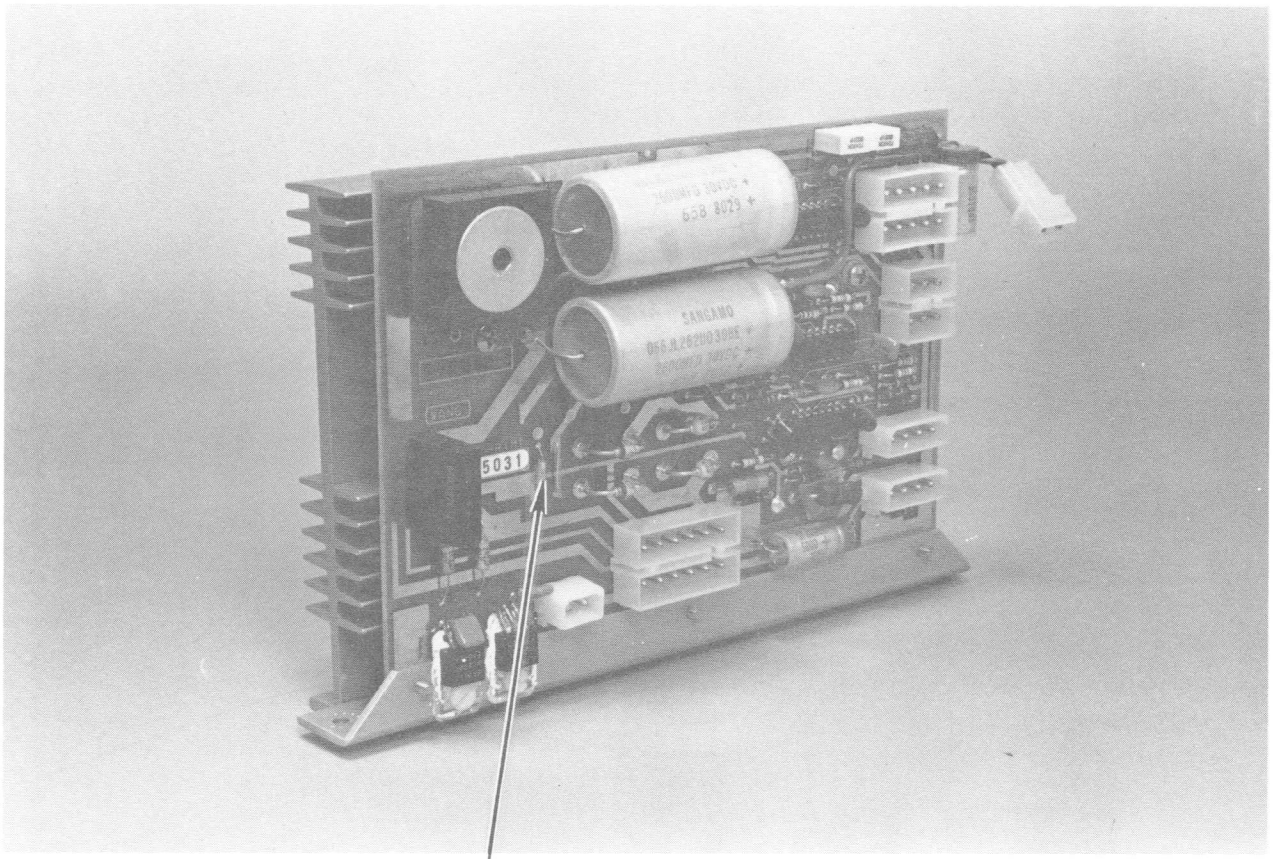


FIGURE 8-22 POWER SUPPLY REGULATOR AND HEAT SINK ASSEMBLY (ITEM 1.10.3)

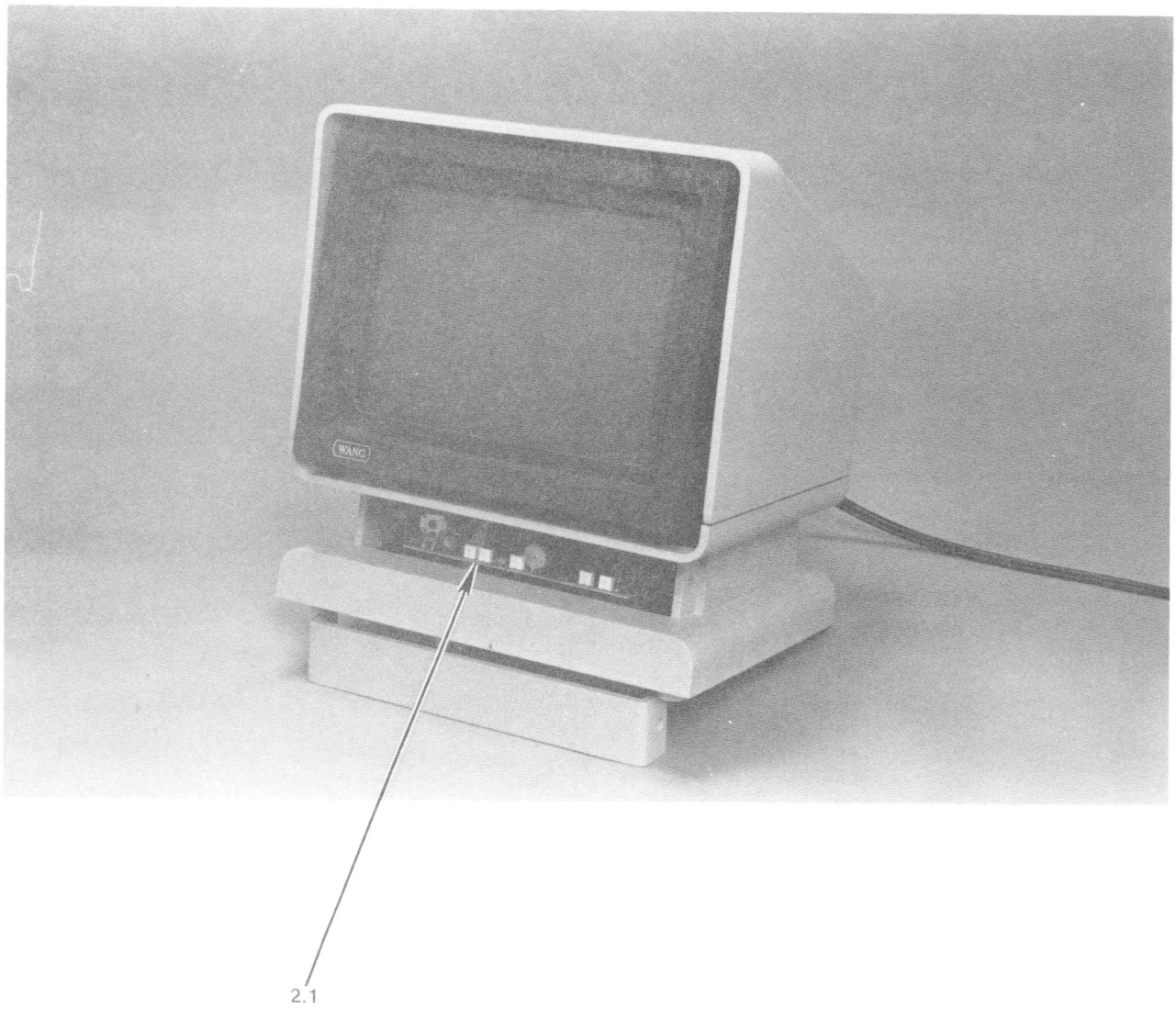


FIGURE 8-23 MONITOR MODULE (ITEM 2.0)

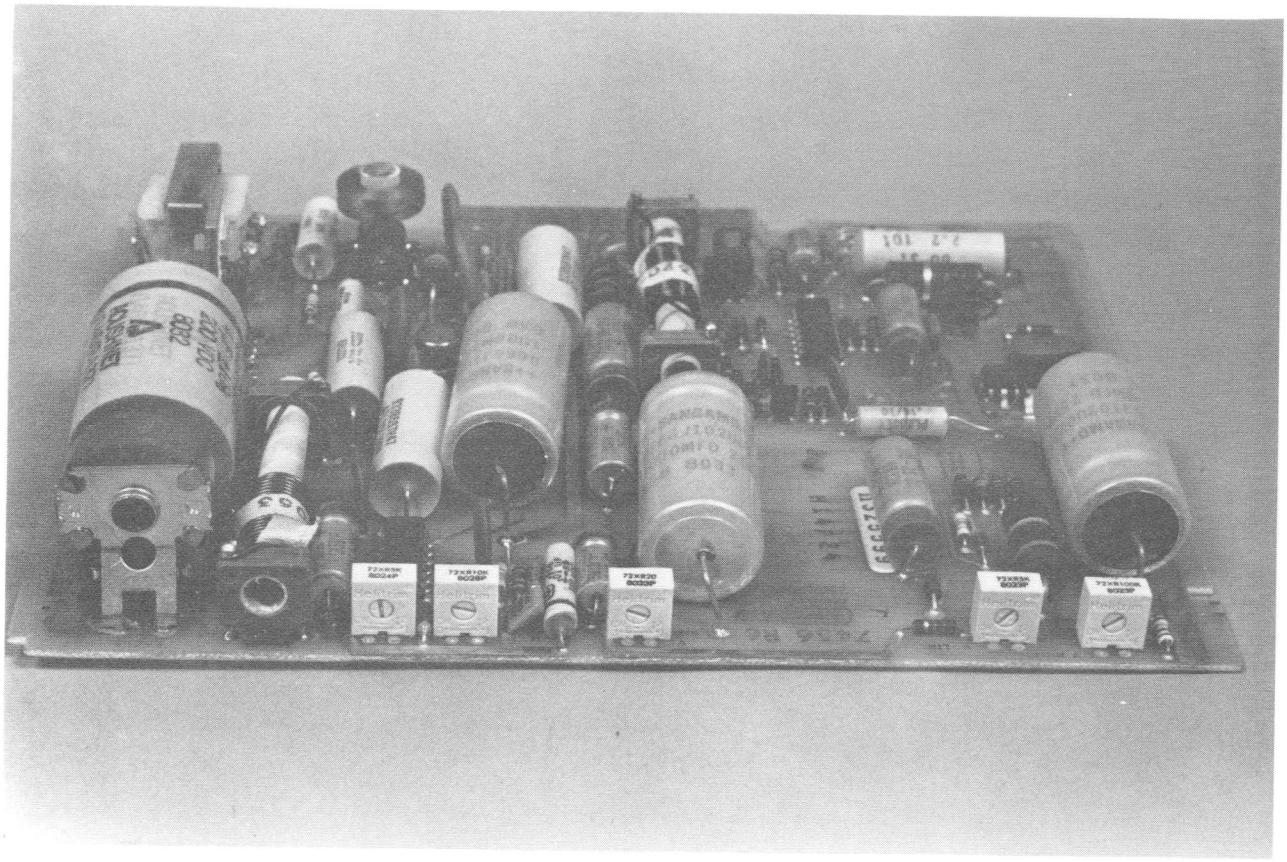


FIGURE 8-24 CRT ELECTRONICS PCA (ITEM 2.1), PERSPECTIVE VIEW

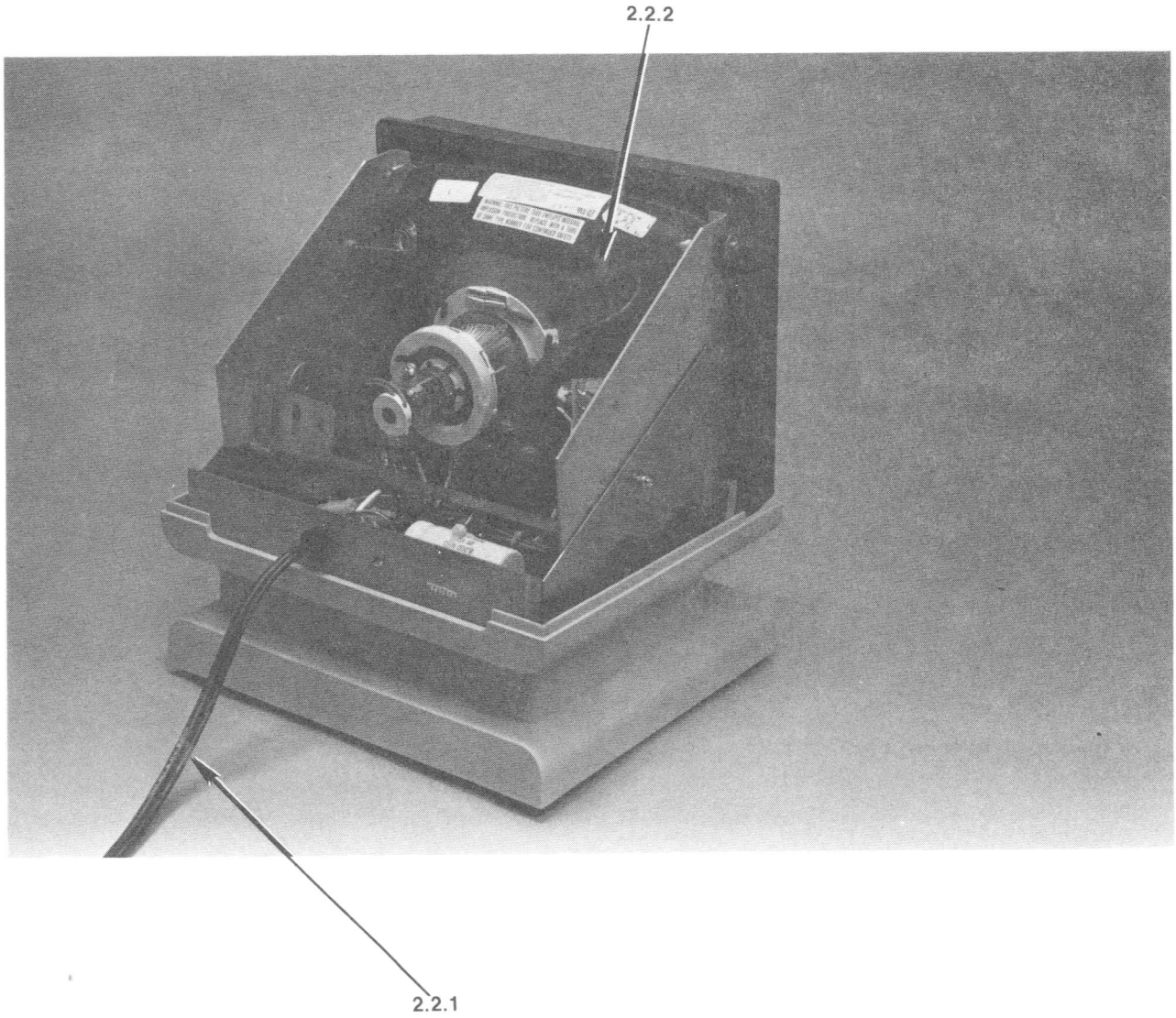


FIGURE 8-25 12-INCH MONITOR & FRAME ASSEMBLY (ITEM 2.2)

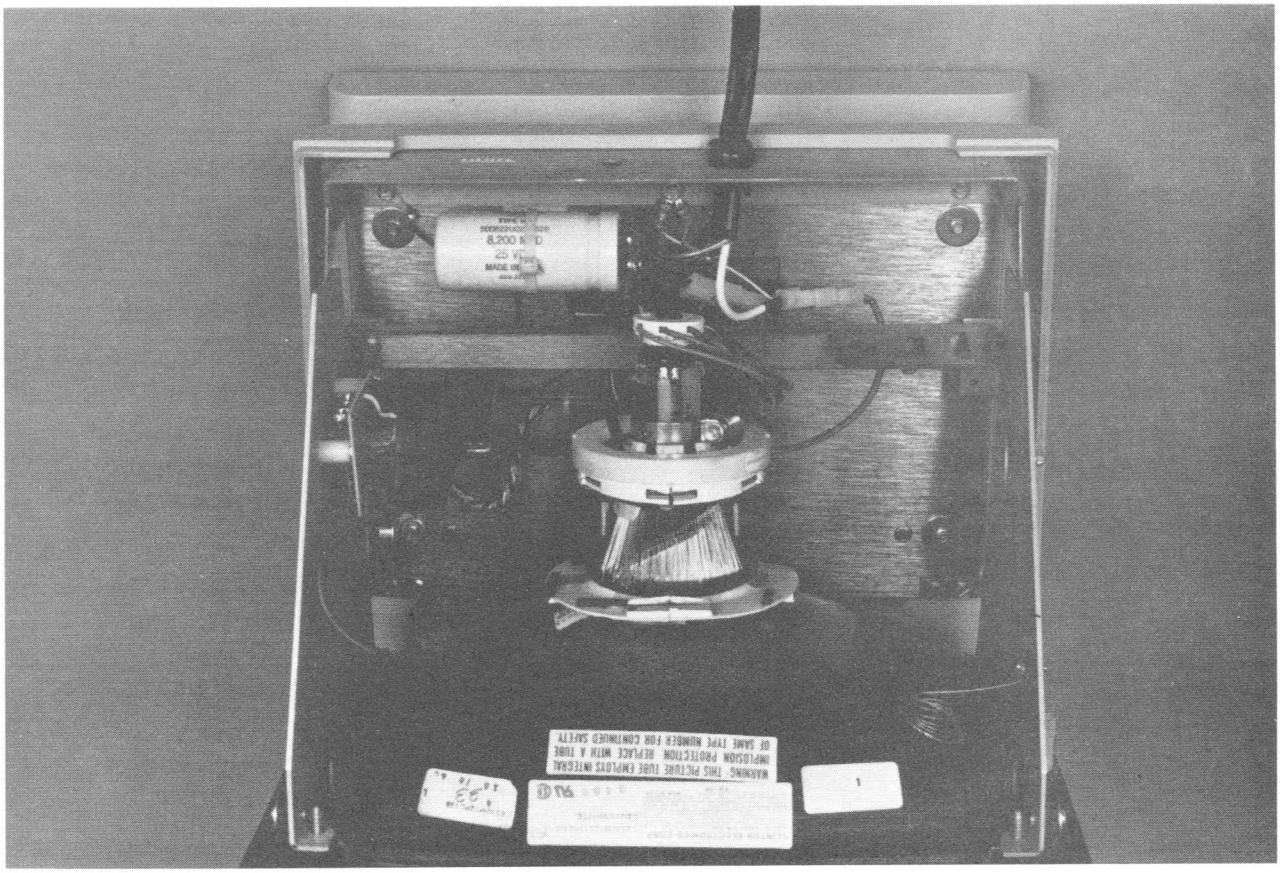


FIGURE 8-26 CRT (ITEM 2.2.2)

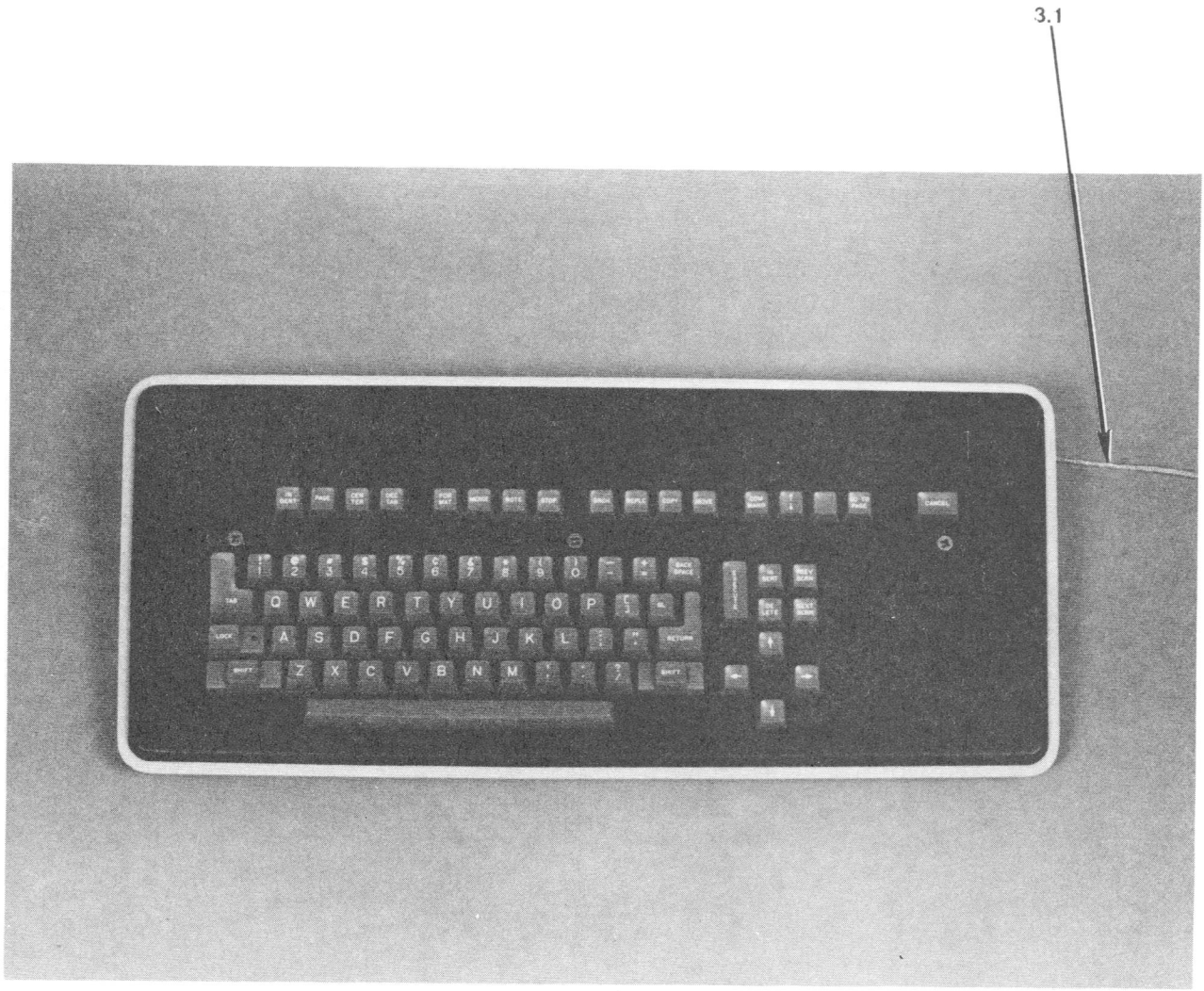


FIGURE 8-27 KEYBOARD MODULE (ITEM 3.0)

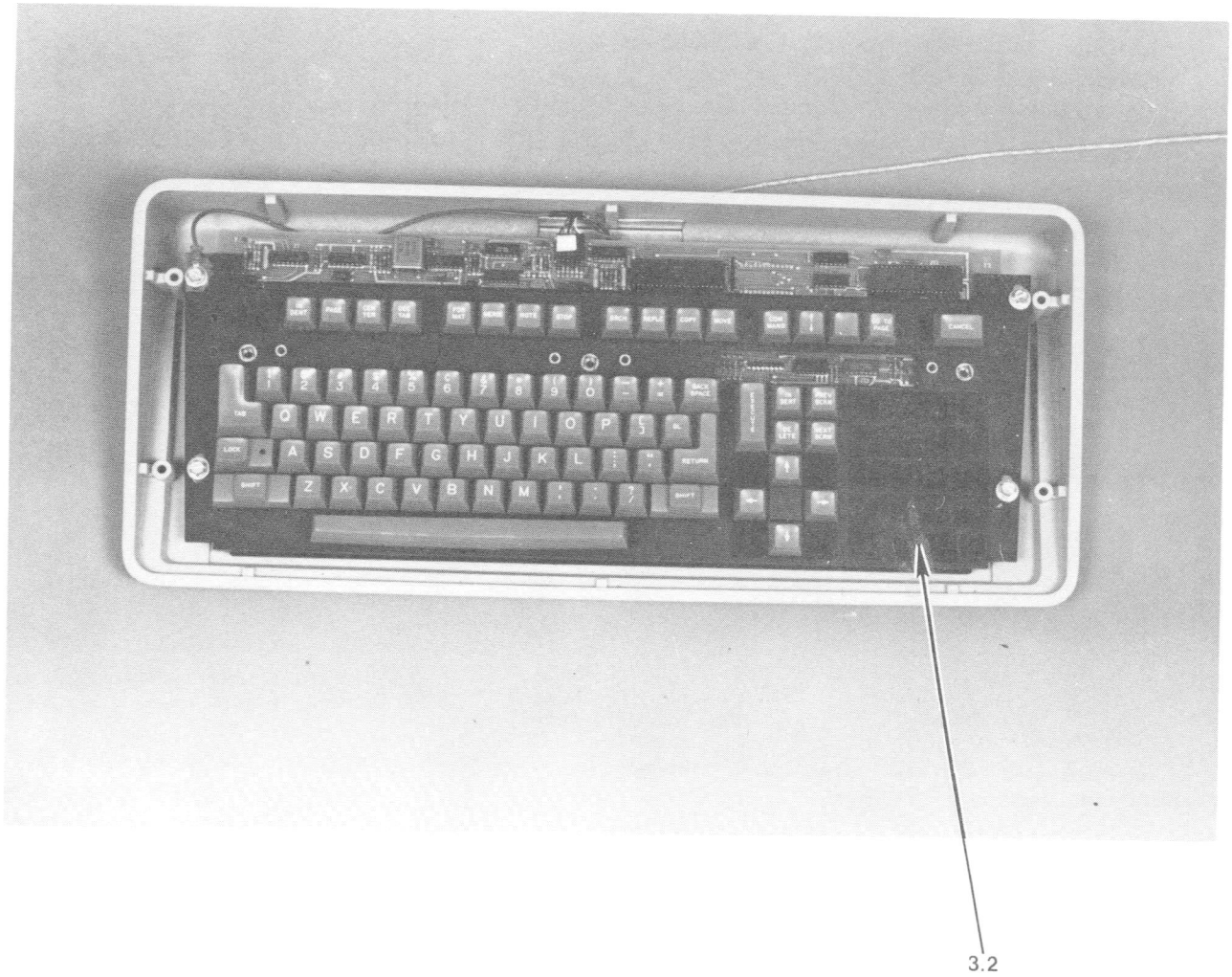


FIGURE 8-28 KEYBOARD ASSEMBLY (ITEM 3.2)

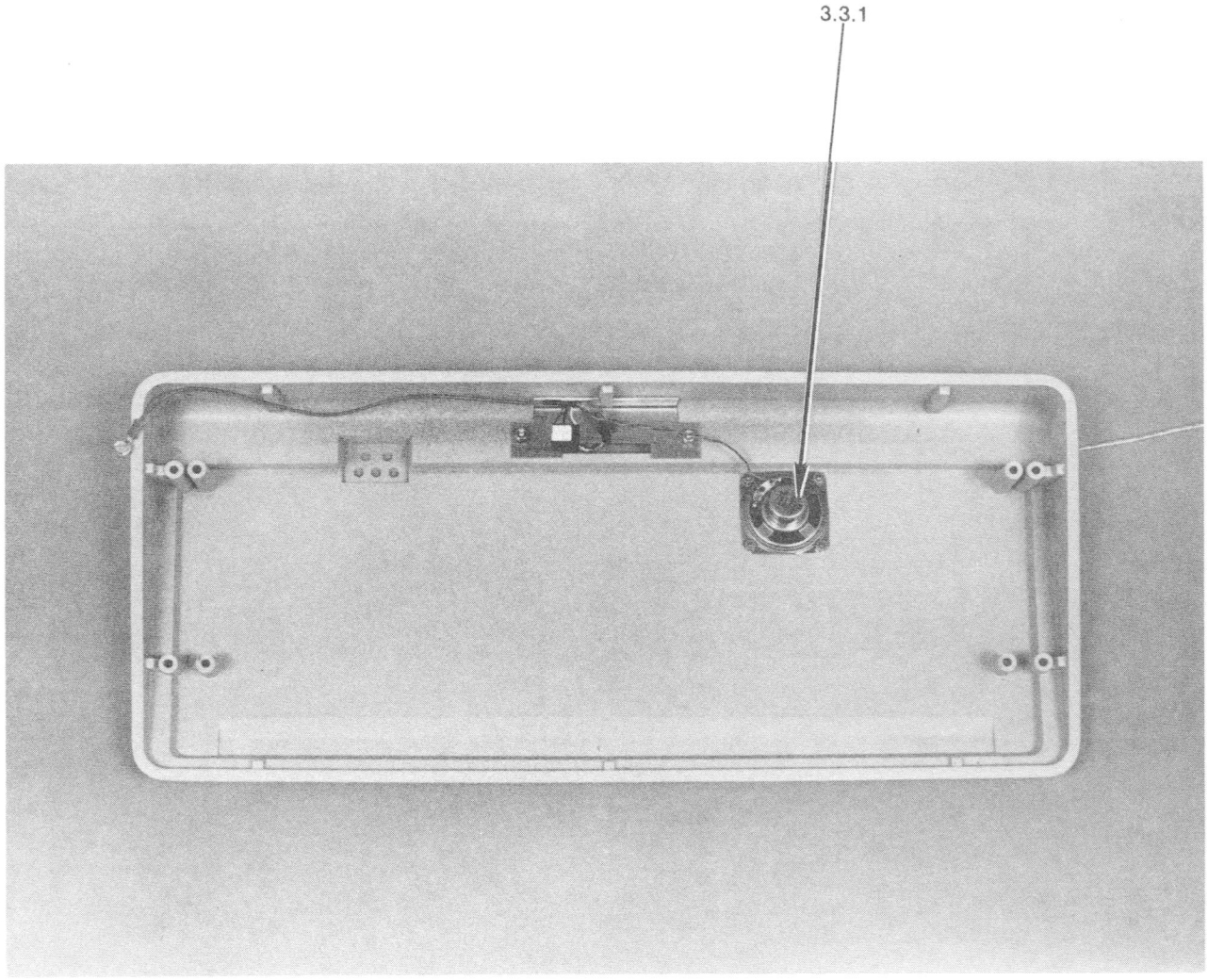


FIGURE 8-29 KEYBOARD BASE (ITEM 3.3)

APPENDIX A
MNEMONICS

Φ	16 Mhz Clock
ΦD	4 Mhz Clock
A0-A7	Addresses
A1/A8	"
A2/A9	"
A3/A10	"
A4/A11	"
A5/A12	"
A6/A13	"
AC0-7	
ALARM	Keyboard Alarm Signal
ARDY	Keyboard Ready Signal
ASTB	Keyboard Strobe Signal
BA0-15	Buffered Address Signals 0 to 15 from Z80 CPU
BA0/C0	
BIORQ	Buffered Input/Output request from Z80 CPU
BM	Buffered Z80 CPU Machine Cycle-One Signal
BMI	
BMREQ	Buffered Memory Request Signal from Z80 CPU
BRD	Buffered Z80 CPU Read Signal
BRFSH	Buffered Z80 Memory Refresh
BUSACK	
BUSRQ	
BWR	Buffered Z80 CPU Write
C HOLD	
C OPEN	
C01-4	
CC0-7	
CHAND	Change Daisy
CHANP	Change Paper
CHANR	Change Ribbon
CLICKER	Keyboard Clicker
CLK GATE	Clock Gate
CP1A-CP1B	

CP2A-CP2B	
CRT RAM SEL	Select CRT RAM Memory
CSYNC	Cursor Sync
D0-7	Data from Z80 Direct
DB0-7	Buffered Data
DIRECTION SEL	Select Direction of Disk Head Carriage
DISK DR	Disk Drive
DISK SELECT	Select Disk for Operation
DK CTRL	Disk Control
DOPT	Device Option
DRIVE SEL 0-1	Select Drive either 0 or 1
ENABLE	Enable Chip
EX CLK	External Clock (diagnostic use)
FAULT	Maintenance Fault
H SYN	Horizontal Synchronization
HAM	Hammer
HGR	Horizontal Graphic
HOME	Home Position
IE0-4	Interrupt Enable Signals
INDEX0-1	Disk Index Pulses (Disk 0 or 1)

V.A.4-M-1

INIT	Initialize
INT	Interrupt
INTEN	Intensity
INTENSITY	
KB CTRL	Keyboard Control
KB DATA	Keyboard Data
L LMT	Left Carriage Limit (Printer)
LD/SH	Load/Shift (Shift Register Control)
LDNSW	Line Down Switch Output Signal
LF DOWN	Line Feed Down (Printer)
LF UP	Line Feed Up (Printer)
LUPSW	Line Up Switch Output Signal
MBREQ	Memory Bus Request
MC	Master Clock
MON0-1	Motor on, 0 or 1 (Disk Drive)
NMI	Non-maskable Interrupt
P CHOP 1	Paper Motor Control Chopped Signal 1
P CHOP 2	" 2
P HOLD	Paper Motor Hold (Brake) Signal
P LOAD	Paper Motor Load Signal
P OUT	
P01-4	
P01-4	
PG0-2	
PLSW	
POR	
PP1A-PP1B	
PP2A-PP2B	
PRNTR	
PSL	
PWR ENABLE	
QC	
QC	

R DOWN
R HOLD
R LMT
R TYPE
R UP
RO1-4
RO1-4
RD DATA
RD DATA
RDNSW
REPEAT
RESET DISK
REVID
RP1A
RP2A
RT
RT
RUPSW
SCO-1
SEL
SELSW
SIDE SELECT
STEP 0-1
STR
STR
TOFSW
TRACK

APPENDIX B
VTAC(R)
CRT VIDEO TIMER-CONTROLLER
(5027)

The CRT Video Timinger-Controller Chip (VTAC)(R) is a user programmable 40-pin COPLAMOS(R) channel MOS/LSI device containing the logic function required to generate all the timing signals for the presentation and formatting of non-interlaced (for MWPS application) video data on a standard or non-standard CRT monitor. See Figure B-1 for a block diagram presentation.

With the exception of the dot counter, which may be clocked at video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by the loading of seven 8-bit control registers directly off an 8-bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self-loaded" via an external PROM tied on the data bus. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

B-2 OPERATION

The design philosphy employed allows the device to interface effectively with either a microprocessor-based or hardwire-logic system. The user programs the device in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. Seven 8-bit words are required to fully program the chip. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3-bit code providing 8 mask programmable character lengths from 20 to 132. The standard device is masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2-bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode-scans/frame = 2X + 513. Therefore for 525 scans, program X=6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range=513 to 1023 scrans/frame = 2X + 256. Therefore for 262 scans, program X=3(00000011). Range=256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (=3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

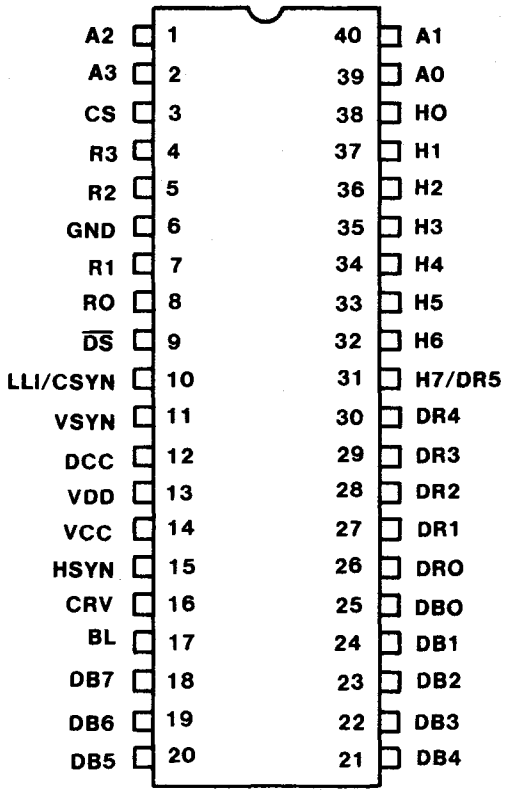
The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's(R) vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's(R) specified logic levels, is applied to the line lock input. The VTAC's(R) inhibit generation of vertical sync until a zero-to-one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.

B-1 PIN INFORMATON

See Figure B-2 for pin-layout information. Table B-1 describes respective pin functions.

TABLE B-1

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
25-18	DB0-7	Data Bus	I/O	Data bus. Input bus for control words from miniprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that is being addressed.
39,40, 1,2	A0-3	Register Address	I	Register address bits for selecting one of seven control registers of either of the cursor address registers.



PACKAGE: 40-PIN D.I.P.

FIGURE B-2 PIN CONFIGURATION

Table B-1 (Continued)

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
26-30	DR0-4	Data Row Counter Outputs	O	Data row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN/ LLI	Composite Sync Ouput/Line Lock Input	O/I	Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057,this pin is the Line Lock Input. The frequency waveform, processed to conform to the VTAC's(R) specified logic levels, is applied to this pin.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	Vcc	Power Supply	PS	+5 volt Power Supply
13	Vdd	Power Supply	PS	+12 volt Power Supply

Table B-1 (Continued)

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
9	DS	Data Strobe	I	Strobes DB0-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus.
12	DCC	DOT Counter Carry	I	Carry from off chip counter establishing basic character clock rate. Character clock.
38-32	H0-6	Character Counter Outputs	O	Character Counter outputs.
7,5,4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line counter (REG.0) is 128; otherwise output is MSB of Data Row Counter.
8	R0	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, R0 will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, R0 will toggle at the data row rate.

APPENDIX C
UPD 765
FLOPPY DISK CONTROLLER

The UPD 765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The UPD 765 provides control signals which simplify the design of an external phase-locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand shaking signals are provided in the UPD 765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the UPD 8257. The FDC operates in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the UPD 765 and DMA controller.

There are 15 separate commands which the UPD 765 executes. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The commands consists of the following.

Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate (Restore to Track 0)
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format a Track	Sense Drive Status

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user.

C-1 PIN INFORMATION

See Figure C-1 for pin-layout information. Table C-1 describes respective pin functions.

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION FROM DMA:
1	RST	Reset	Input	From processor: Places FDC in idle state. Resets output lines to FDD to "0" (low)
2	RD	Read	Input(1)	From Processor: Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	WR	Write	Input(1)	From Processor: Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	CS	Chip Select	Input	From Processor: IC selected when "0" (low), allowing RD and WR to be enabled.
5	A_0	Data/Status Reg Select	Input(1)	From Processor: Selects Data Reg (A_0) contents of the FDC to be sent to Data Bus.
6-13	DB_0- DB_7	Data Bus	Input(1) Output	From Processor: Bi-Directional 8-bit Data Bus.
14	DRQ	Data DMA Request	Output	To DMA: DMA Request is being made by FDC when DRQ "1"

NOTE (1) Disabled when CS=1

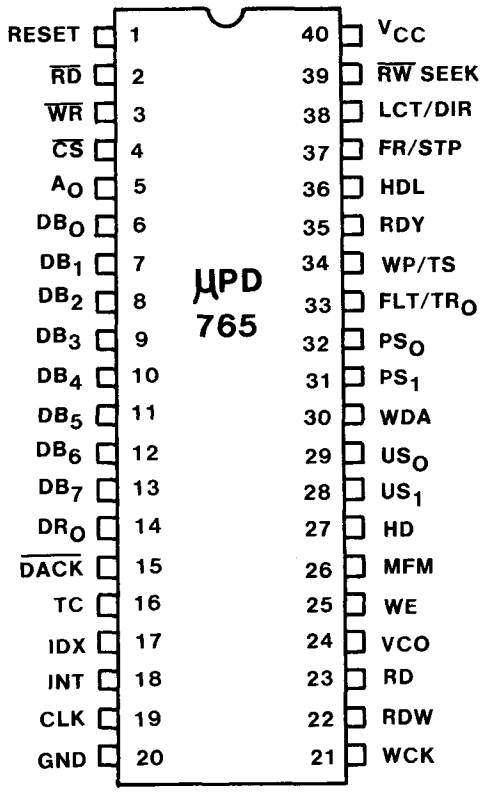


FIGURE C-1 PIN CONFIGURATION

Table C-1 (Continued)

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
15	DACK	DMA Acknowledge	Input	From DMA: DMA cycle is active when "0" (low) and Controller is perform- ing DMA transfer
16	TC	Terminal Count	Input	From DMA: Indicates the termination of a DMA transfer when "1" (High)
17	IDX	Index	Input	From FDD: Indicates the beginning of a disk track
18	INT	Interrupt	Output	To Processor: Interrupt Request Generated by FDC
19	CLK	Clock	Input	Single Phase 8MHz Squarewave Clock
20	GND	Ground		DC Power Return
21	WCK	Write Clock	Input	Write data rate to FDD FM 500kHz MFM 1 MHz with a pulse width of 250ns for both FM and MFM.
22	RDW	Read Data Window	Input	Generated by PLL and used to sample data from FDD
23	RDD	Read Data	Input	Read data from RDD, containing clock and data bits
24	VCO	VCO Sync	Output	Inhibits VCO in PLL when "0" (low) enables VCO when "1"
25	WE	Write Enable	Output	Enables write data into FDD
26	MFM	MFM Mode	Output	To Phase Lock Loop: MFM mode when "1" FM mode when "0"

Table C-1 (Continued)

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
27	HD	Head Select	Output	To FDD: Head 1 selected when "1" (high). Head 0 selected when "0" (low).
28,29	US_1, US_0	Unit Select	Output	To FDD: FDD Unit Selected
30	WDA	Write Data	Output	To FDD: Serial clock and data bits to FDD
31,32	PS_1, PS_0	Precompensation (pre-shift)	Output	To FDD: Write precomposition status during MFM mode. Determines early, late, and normal times.
33	FLT/ TR_0	Fault/Track 0	Input	From FDD: Senses FDD fault condition, in Read/Write mode and Track 0 condition in Seek mode
34	WP/TS	Write Protect/ Two-side	Input	From FDD: Senses Write Protect status in Read/Write mode, and Two-Side Media in Seek mode.
35	RDY	Ready	Input	From FDD: Indicates FDD is ready to send or receive data
36	HDL	Head Load	Output	To FDD: Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	Output	To FDD: Resets fault FF in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode

38	LCT/ DIR	Low current/ Direction	Output	To FDD: Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode.
39	RW/ SEEK	Read Write/ SEEK	Output	To FDD: When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V		D.C. Power

C-2 PROCESSOR INTERFACE

The UPD 765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the UPD 765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it has been instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

During Command or Result Phases the Main Status Register (See Figure C-2) must be read by the processor (See Figure C-3 & C-4) before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the UPD 765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the UPD 765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before each byte is read from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the uPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

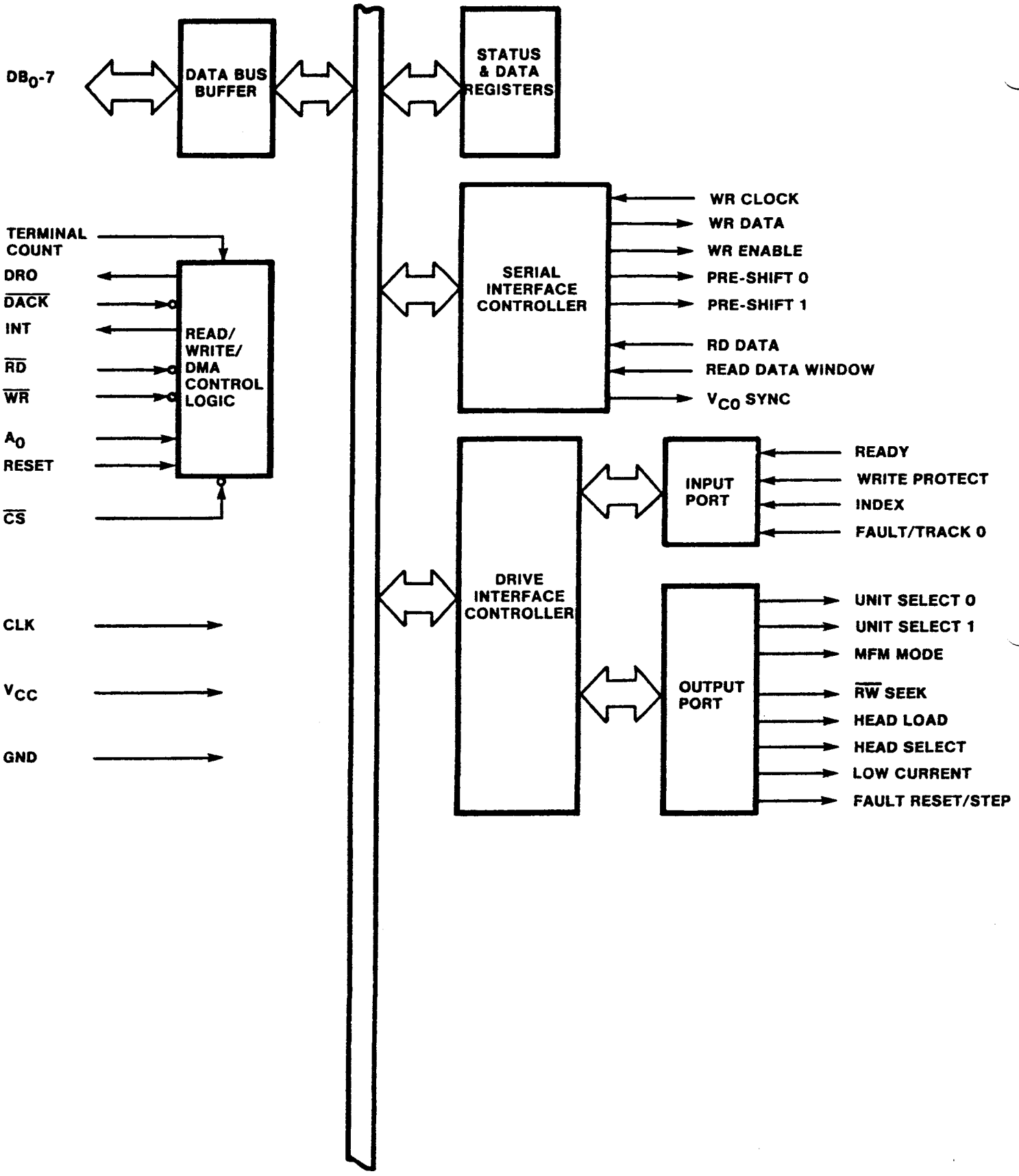


FIGURE C-2 μPD765 BLOCK DIAGRAM

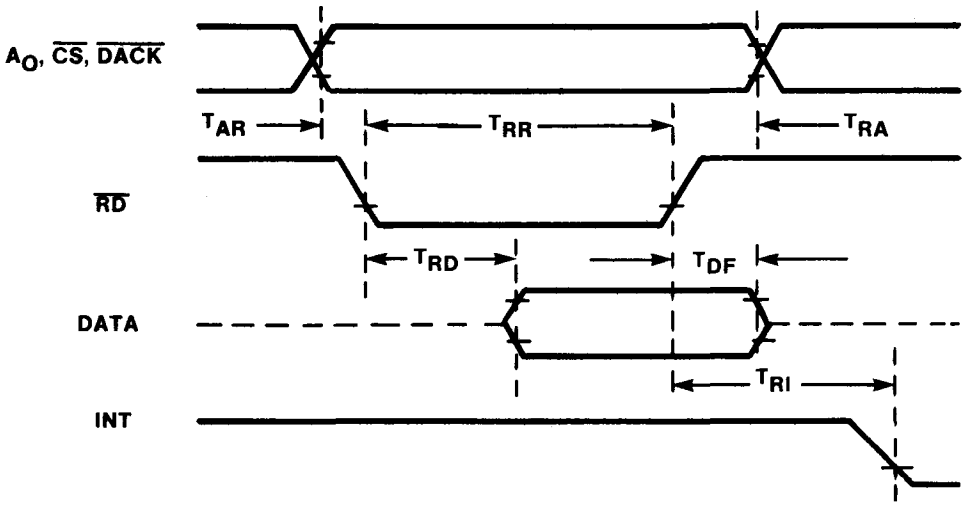


FIGURE C-3 PROCESSOR READ OPERATION

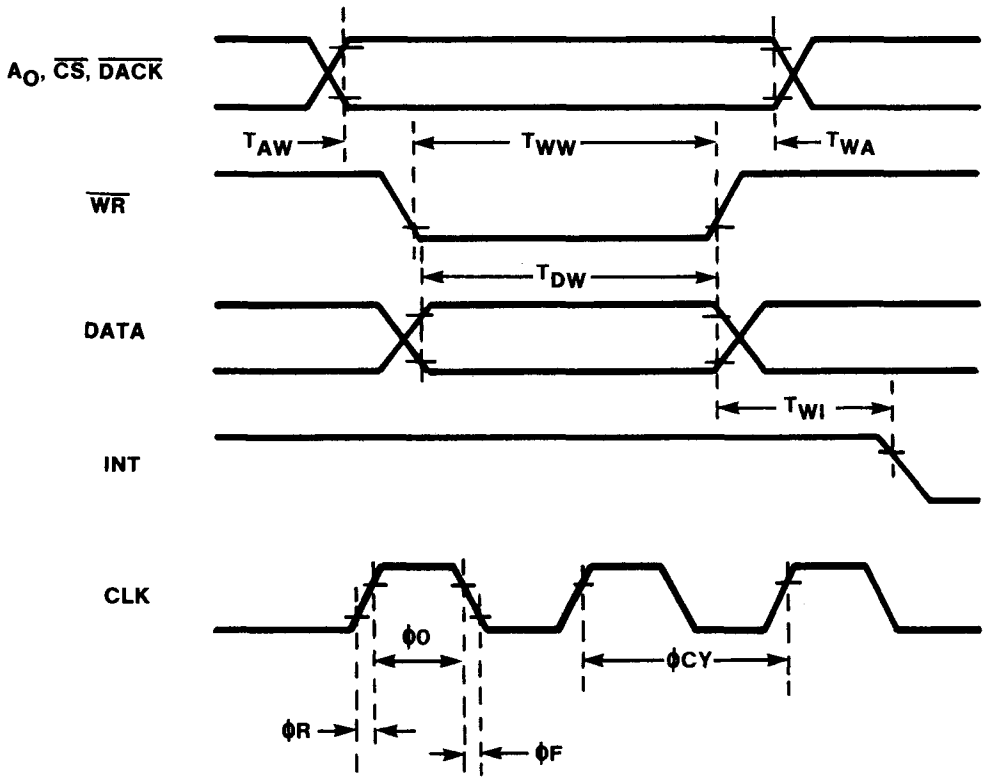


FIGURE C-4 PROCESSOR WRITE OPERATION

During the Execution Phase, the Main Status Register need not be read. If the UPD 765 is in the NON-DMA Mode, then the receipt of each data byte (if UPD 765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT=1). The generation of a Read signal (RD=0) will reset the interrupt as well as output the Data onto the Data Bus. If the processor cannot handle interrupts fast enough (every 13 us), it may poll the Main Status Register; bit D7 (RQM) then functions as the Interrupt signal. If a Write Command is in process, the WR signal performs the reset to the Interrupt signal.

If the UPD 765 is in the DMA Mode (See Figure C-5), no Interrupts are generated during the Execution Phase. The UPD 765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a DACK=0 (DMA Acknowledge) and a RD=0 (Read Signal). When the DMA Acknowledge signal goes low (DACK=0), the DMA Request is reset (DRQ=0). If a Write Command has been programmed, a WR signal appears instead of RD. After the Execution Phase has been completed (Terminal Count has occured), an Interrupt occurs (INT=1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT=0).

C-4 SEEK OPERATION

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head postion with the NCN (New Cylinder Number), and if there is a difference performs the following operation.

PCN NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In)

PCN NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out)

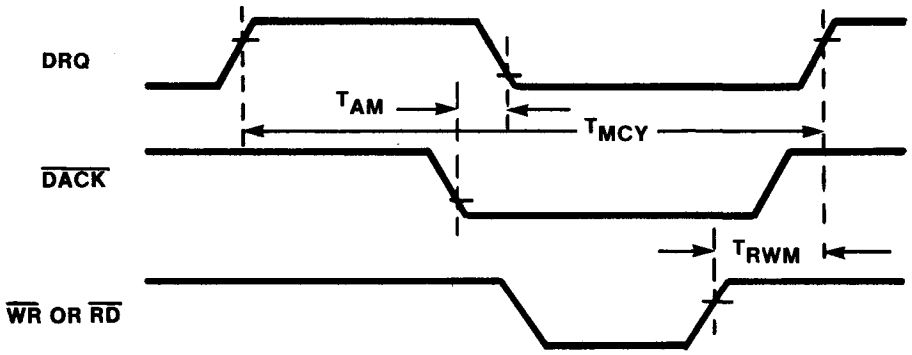


FIGURE C-5 DMA OPERATION

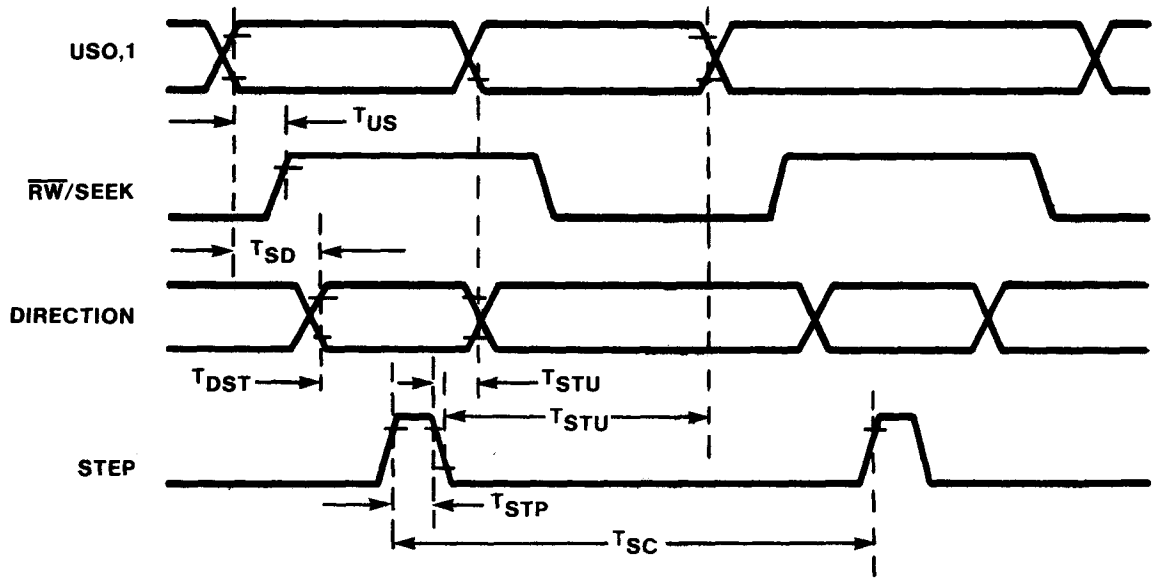


FIGURE C-6 SEEK OPERATION

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN=PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

APPENDIX D

UART/IM6402

This Universal Asynchronous Receiver/Transmitter (UART) provides an asynchronous interface between the keyboard/Ay-3-4592 and the keyboard data output. In the receiving mode, the UART converts serial start data, parity and stop bits to parallel data verifying proper code transmission parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. See Figure D-1 for chip overall block diagram.

D-1 TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmit it in serial form (Figure D-2) on the TROutput terminal.

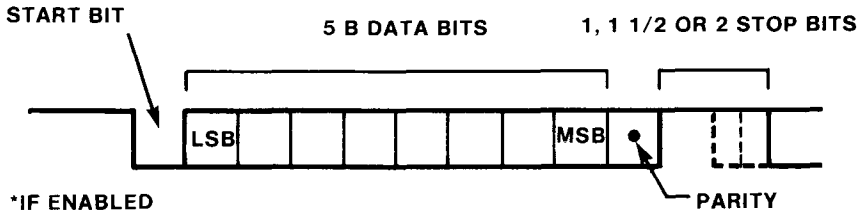
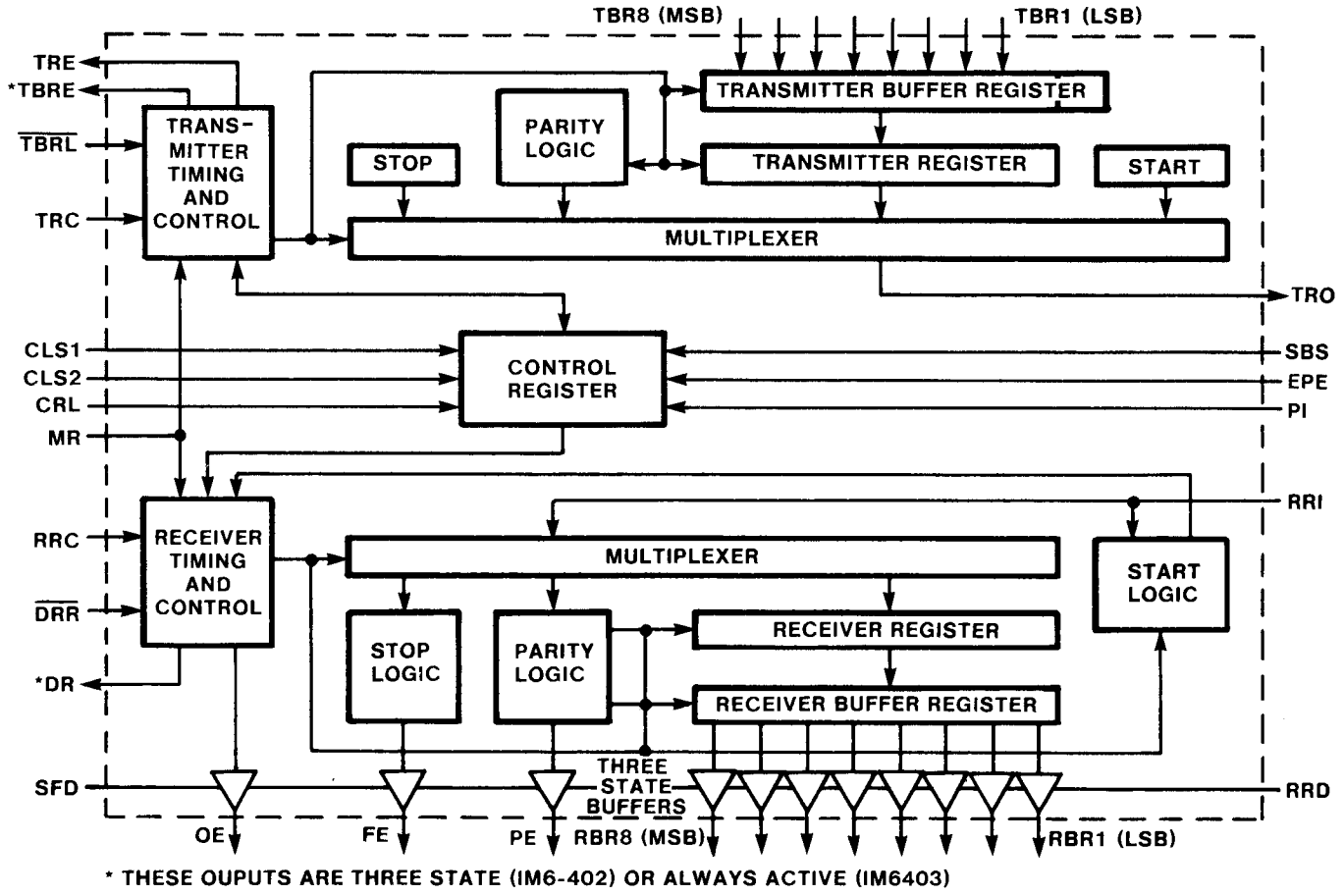


FIGURE D-2 SERIAL DATA

Transmitter timing is shown in Figure D-3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 thrugh TBR8 by a logic low on the TBR Load input. Valid data must be present prior to and following the rising edge of TBRL. If words of less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later data, is transferred to the transmitter register and TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock. The clock rate is 16 times the data rate.



* THESE OUPUTS ARE THREE STATE (IM6-402) OR ALWAYS ACTIVE (IM6403)

FIGURE D-1 IM6402/03 FUNCTIONAL BLOCK DIAGRAM

(C) A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register, and transmission of the character begins.

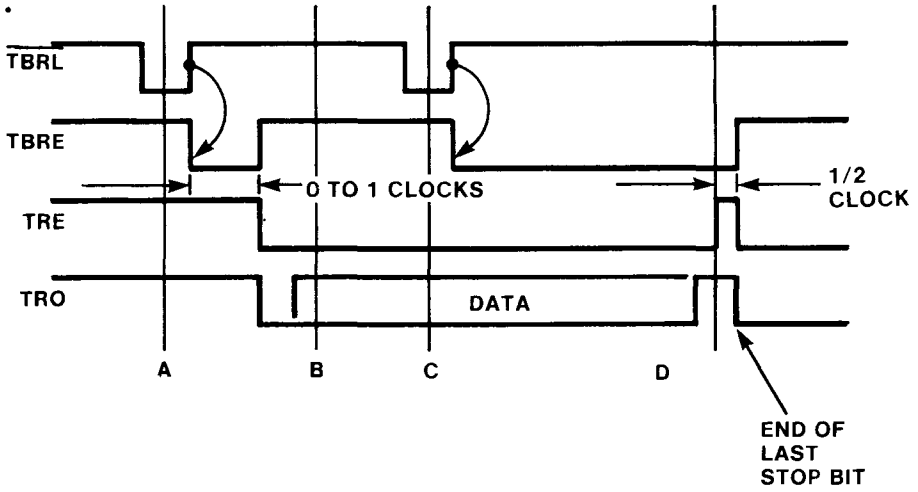


FIGURE D-3 TRANSMITTER TIMING (NOT TO SCALE)

D-2 RECEIVER OPERATION

Data is received in serial form at the R1 input. When no data is being received R1 input must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Receiver timing is shown in Figure D-4.

(A) A low level on DRReset clears the DReady line. (B) During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits the unused most significant bits are at logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character is transferred to the RBRegister. A logic high on PError indicates a parity error. (C) 1/2 clock cycle later DRready is set to a logic high and FError is evaluated. A logic high on FError indicates that an invalid stop bit has been received. The receiver does not begin searching for the next start bit until a stop bit is received.

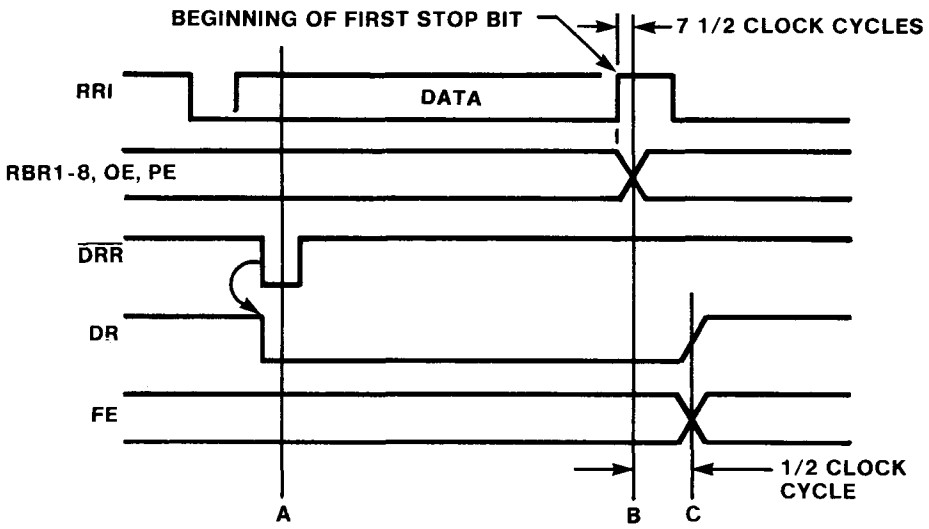


FIGURE D-4 RECEIVER TIMING (NOT TO SCALE)

D-3 START BIT DETECTION

(B) The receiver uses a 16X clock for timing (see Figure D-5). The start bit (A) may occur as much as one clock cycle before it is detected as indicated by the shaded portion. The center of the start bit is defined as clock count 7-1/2. If the receiver clock is a symmetrical square wave, the center of the start is be located within $\pm$1/2 clock cycle $\pm$ 1/32 bit or $\pm$3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

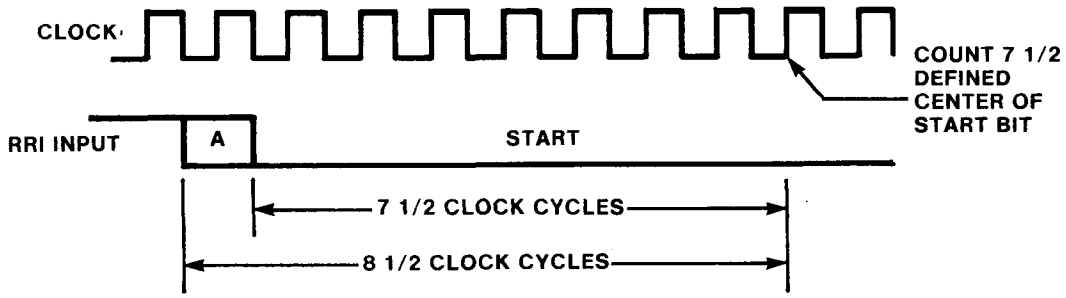


FIGURE D-5 START BIT TIMING

D-4 PIN INFORMATION

See Figure D-6 for pin identification. Table D-1 describes respective pin functions.

Table D-1. Pin Functional Descriptions

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402 N/C IM6403 Control	No connection Divide Control High 2^4 (16) Divider Low 2^{11} (2048) Divider
3	GND	A high level on RECEVER REGISTER DISABLE forces the receiver holding register outputs RBR1. RBR8 to a high impedance state.
4	RRD	The contents of the RECEIVER BUFFER REGISTER appear on these three state outputs Word formats less than 8 characters are right justified to RBR1.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appears on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See pin 5 - RBR8
7	RBR6	See pin 5 - RBR8
8	RBR5	See pin 5 - RBR8

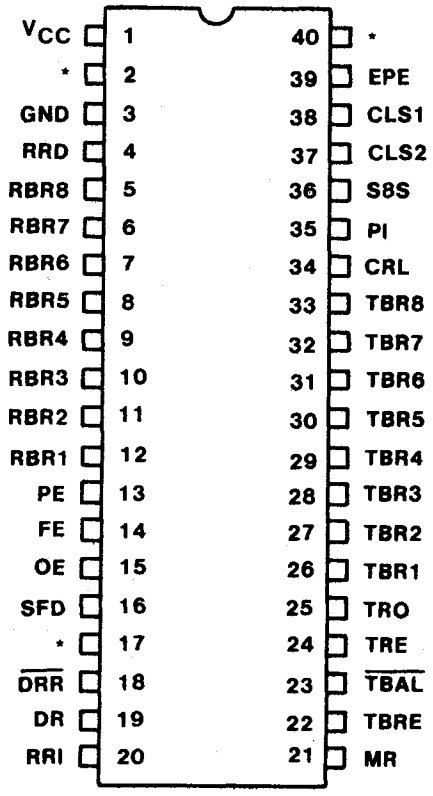


FIGURE D-6 PIN CONFIGURATION

Table D-1 (Continued)

PIN	SYMBOL	DESCRIPTION
9	RBR4	See pin 5 - RBR8
10	RBR3	See pin 5 - RBR8
11	RBR2	See pin 5 - RBR8
12	RBR1	See pin 5 - RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is unhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE stays active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e. DRR active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.

Table D-1 (Continued)

PIN	SYMBOL	DESCRIPTION
17	IM6402-RRC	The RECEIVER REGISTER CLOCK IS 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates that the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.

Table D-1 (Continued)

PIN	SYMBOL	DESCRIPTION
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low-to-high transition on TBRL requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7 and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See pin 26 - TBR1
28	TBR3	See pin 26 - TBR1
29	TBR4	See pin 26 - TBR1
30	TBR5	See pin 26 - TBR1

Table D-1 (Continued)

PIN	SYMBOL	DESCRIPTION
31	TBR6	See pin 26 - TBR1
32	TBR7	See pin 26 - TBR1
33	TBR8	See pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	P1	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bit for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5-bits) CLS1 high CLS2 low 8-bits) CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When P1 is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

APPENDIX E

CTC

Z80-COUNTER TIMER CIRCUIT

The Z80-Counter Timing Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packed in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock. Major features of the Z80-CTC include:

- All inputs and outputs fully TTL compatible.
- Each channel may be selected to operate in either Counter Mode or Timer Mode.
- Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero.
- A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode.
- Selectable positive or negative initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.
- Interrupts may be programmed to occur on the zero count condition in any channel.
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic.

A block diagram of the Z80-CTC is shown in Figure E-1. The internal structure of the Z80-CTC consists of a Z80-CPU bus interface, Internal Control Logic, four sets of Counter/Timer Channel Logic, and Interrupt Control Logic. The four independent counter/timer channels are identified by sequential numbers from 0 to 3. The CTC has the capability of generating a unique interrupt vector for each separate channel (for automatic vectoring to an interrupt service routine). The 4 channels can be connected into four contiguous slots in the standard Z80 priority chain with channel number 0 having the highest priority. The CPU bus interface logic allows the CTC device to interface directly to the CPU with no other external logic. However, port address decoders and/or line buffers may be required for large systems.

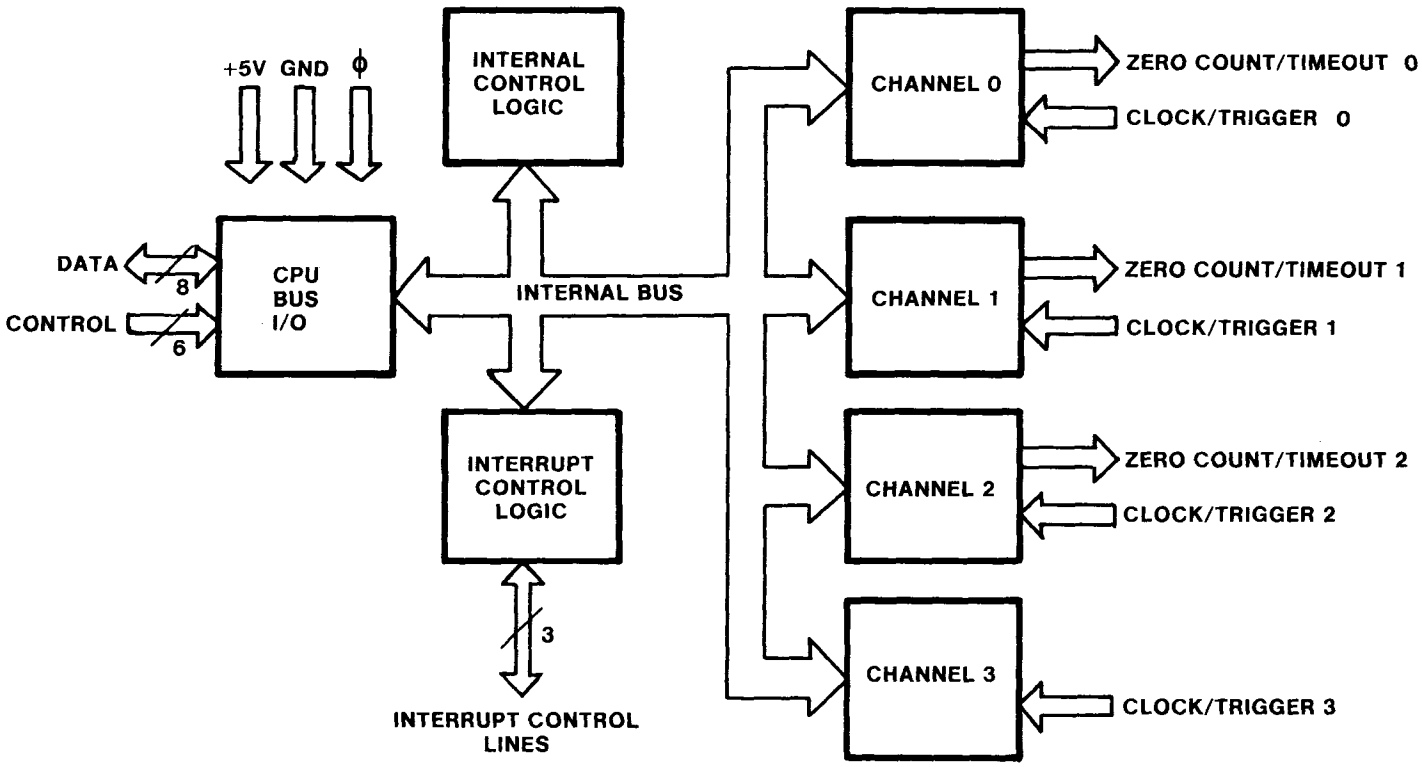


FIGURE E-1 CTC BLOCK DIAGRAM

E-1 CHANNEL LOGIC

The structure of one of the four sets of Counter/Timer Channel Logic is shown in Figure E-2. This logic consists of 2 registers, 2 counters and control logic. The registers are an 8-bit Time Constant Register and an 8-bit Channel Control Register. The counters are an 8-bit CPU-readable Down Counter and an 8-bit Prescaler.

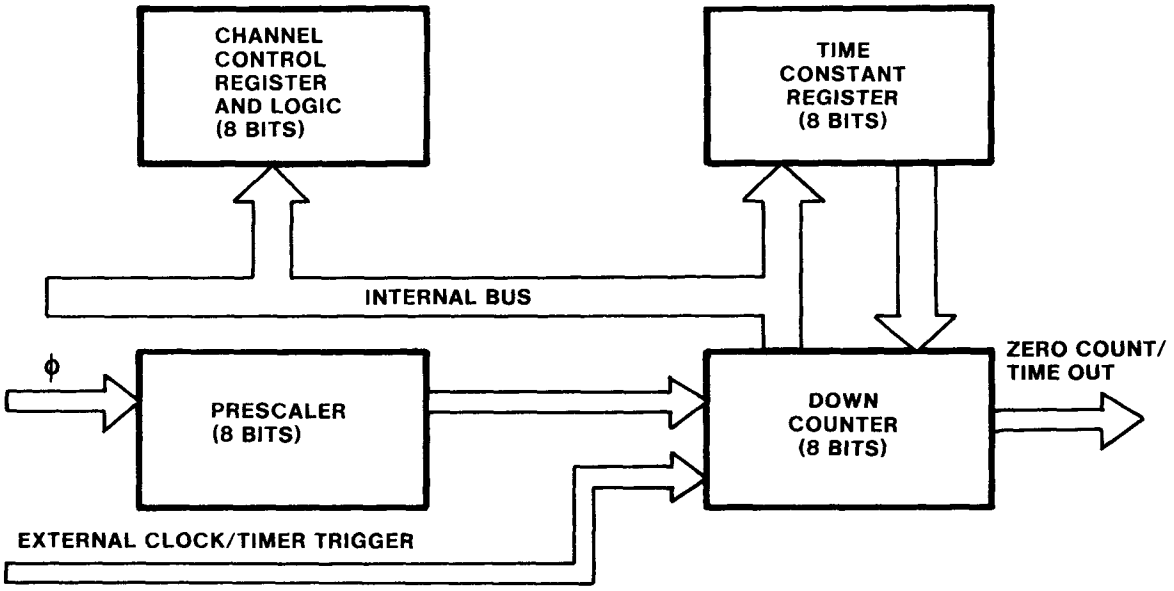


FIGURE E-2 CHANNEL BLOCK DIAGRAM

The Channel Control Register (8-bit) and Logic is written to by the CPU to select the modes and parameters of the channel. Within the entire CTC device there are four such registers, corresponding to the four Counter/Timer Channels. Which of the four is being written to depends on the encoding of two channel select input pins: CS0 and CS1 (usually attached to A0 and A1 of the CPU address bus). This is illustrated in the truth table below:

	CS1	CS0
CH0	0	0
CH1	0	1
CH2	1	0
CH3	1	1

In the control word written to program each Channel Control Register, bit 0 is always set, and the other 7 bits are programmed to select alternatives on the channel's operating modes and parameters, as shown in Figure E-3.

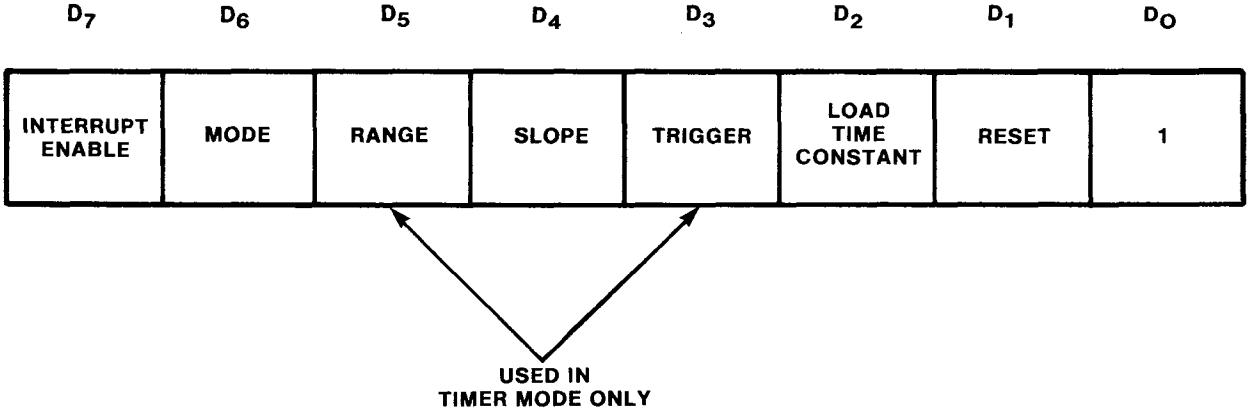


FIGURE E-3 CHANNEL CONTROL REGISTER

Used in the Timer Mode only, the Prescaler is an 8-bit device which can be programmed by the CPU via the Channel Control Register to divide its input, the System Clock, by 16 or 256. The output of the Prescaler is then fed as an input to clock the Down Counter, which initially, and every time it clocks down to zero, is reloaded automatically with the contents of the Timer Constant Register. In effect this again divides the System Clock by an additional factor of the time constant. Every time the Down Counter counts down to zero, its output, Zero Count/Timeout (ZC/TO), is pulsed high.

The Time Constant Register is an 8-bit register, used in both Counter Mode and Timer Mode, programmed by the CPU just after the Channel Control Word with an integer time constant value of 1 through 256. This register loads the programmed value into the Down Counter when the CTC is first initialized and reloads the same value into the Down Counter automatically whenever it counts down thereafter to zero. If a new time constant is loaded into the Time Constant Register while a channel is counting or timing, the present down count will be completed before the new time constant is loaded into the Down Counter.

The Down Counter is an 8-bit register, used in both Counter Mode and Timer Mode, loaded initially, and later when it counts down to zero, by the Time Constant Register. The Down Counter is decremented by each external clock edge in the Counter Mode, or in the Timer Mode, by the clock output of the Prescaler. At any time, by performing a simple I/O Read at the port address assigned to the selected CTC channel, the CPU can access the contents of this register and obtain the number of counts-to-zero. Any CTC channel may be programmed to generate an interrupt request sequence each time the zero count is reached.

In channels 0, 1, and 2, when the zero count condition is reached, a signal pulse appears at the corresponding ZC/TO pin. Due to package pin limitations, however, channel 3 does not have this pin and so may be used only in applications where this output pulse is not required.

E-2 PIN DESCRIPTION

See Table E-1 for a function description of chip input/output pins.

Table E-1. CTC Pin Functional Description

PIN NO.	SYMBOL	INPUT/ OUTPUT	FUNCTION
4-1, 28-25	DB7-DB0	I/O	For transfer of all data and commands.
19. 18	CS1, CS0	I	Two-bit address for selecting one of the four CTC channels.
16	CE	I	Enables the CTC to accept inputs from the Z80 data bus during an I/O write cycle, or to transmit the contents of the down counter to the CPU during an I/O read cycle.

Table E-1 (continued)

PIN NO.	INPUT/ SYMBOL	OUTPUT	FUNCTION
15	Sys Clk	I	Synchronize certain signals internally.
14	M1	I	Machine-cycle 1 from CPU. With both M1 and RD active, the CPU fetches an instruction from memory. With M1 and RD active, the CPU fetches an instruction from memory. With M1 and IORQ active, the CPU acknowledges an interrupt alerting the CTC to place an interrupt vector on the Z80 data bus.
10	IORQ	I	Input/output request from CPU.
6	RD	I	In conjunction with the IORQ and CE signals, transfer data and channel-control words between the CPU and the CTC. During a CTC write cycle, IORQ and CE must be true and RD false.
13	IEI	I	Interrupt Enable In: Helps form a system-wide interrupt daisy chain establishing priorities when more than one peripheral device has interrupt capability. A high indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the CPU.

Table E-1 (continued)

11	IEO	O	Interrupt Enable Out: In conjunction with IEI, forms a system-wise interrupt priority daisy chain. IEO is high only if IEI is high, AND THE CPU is not servicing an interrupt from any CTC channel.
12	INT	O	Goes true when any CTC channel programmed to enable interrupts has a zero-count in its down counter.
17	RESET	I	Stops all channels from counting and resets channel interrupt enable bits in all control registers, thereby disabling CTC-generated interrupts. The CTC data bus output drives go to the high impedance state.
20, 21, 22, 23	CLK/TRG3 thru CLK/TRG0	I	Four CLK/TRG pins corresponding to the four independent CTC Channels. In counter mode, each active edge decrements the down counter. In the timer mode, an active edge initiates the timing function.
9, 8, 7	ZC/TO2	O	There are three ZC/TO pins corresponding to CTC channels 2 thru 0 (Due to package limitations, channel 3 has no ZC/TO pin). In either counterrrrmode or timer mode, when the down counter decrements to zero, an active high-going pulse appears at the respective associated pin.

E-3 COUNTER MODE

At power-on, the Z80-CTC state is undefined. Asserting RESET puts the CTC in a known state. Before any counting or timing can begin, a Channel Control Word and a time constant data word must be written to the appropriate registers of that channel. Further, if any channel has been programmed to enable interrupts, an Interrupt Vector word must be written to the CTC's Interrupt Control Logic. (For further details, refer to section 5.0: "CTC Programming.") When the CPU has written all of these words to the CTC all active channels will be programmed for immediate operation in either the Counter Mode or the Timer Mode

In the counter mode (See Figure E-4) the CTC counts edges of the CLK/TRG input. The Counter Mode is programmed for a channel when its Channel Control Word is written with bit 6 set. The Channel's External Clock (CLK/TRG) input is monitored for a series of triggering edges; after each, in synchronization with the next rising edge of (the System Clock), the Down Counter (which is initialized with the time constant data word at the start of any sequence of down-counting) is decremented. Although there is not set-up time requirement between the triggering edge of the External Clock and the rising edge of system clock, the Down Counter will not be decremented until the following pulse. A channels's External clock input is pre-programmed by bit 4 of the Channel Control Word to trigger the decrementing sequence with either a high or a low going edge.

In any of Channels 0, 1, or 2, when the Down Counter is successively decremented from the original time constant until finally it reaches zero, the Zero Count (ZC/TO) output pin for that channel is pulsed active (high). (However, due to package pin limitations, channel 3 does not have this pin and so may only be used in applications where this output pulse is not required.) Further, if the channel has been so pre-programmed by bit 7 of the Channel Control Word, an interrupt request sequence will be generated.

As the above sequence is proceeding, the zero count condition also results in the automatic reload of the Down Counter with the original time constant data word in the Time Constant Register. There is no interruption in the sequence of continued down-counting. If the Time Constant Register is written to with a new time constant data word while the Down Counter is decrementing, the present count will be completed before the new time constant is loaded into the Down Counter.

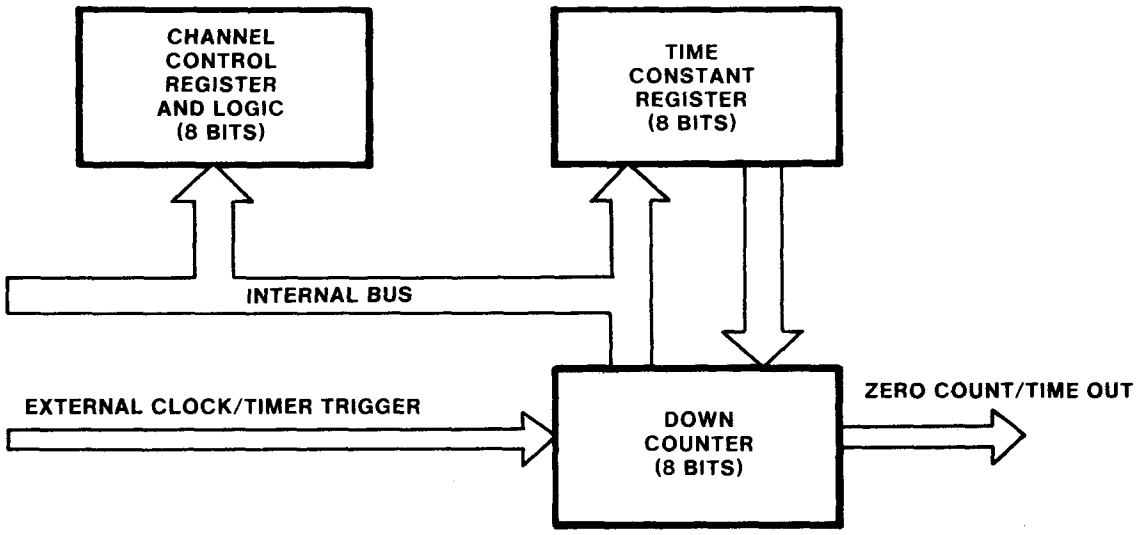


FIGURE E-4 CHANNEL-COUNTER MODE

E-4 TIMER MODE

In this mode (See Figure E-5), the CTC generates timing intervals that are an integer value of the sytem clock period. The Timer Mode is programmed for a channel when its Channel Control Word is written with bit 6 reset. The channel than may be used to measure intervals of time based on the System Clock period. The System Clock is fed through two successive counters, the Prescaler and the Down Counter. Depending on the pre-programmed bit 5 in the Channel Control word, the Prescaler divides the System Clock by a factor of either 16 or 256. The output of the Prescaler is then used as a clock to decrement the Down Counter, which may be pre-programmed with any time constant integer between 1 and 256. As in the Counter Mode, the time constant is automatically reloaded into the Down Counter at each zero-count condition, and counting continues. Also at zero-count, the channel's Time Out (ZC/TO) output (which is the output of the Down Counter) is pulsed, resulting in a uniform pulse train of precise period given by the product.

$$t_c * P * TC$$

where t_c is the System Clock period, P is the Prescaler factor of 16 or 256 and TC is the pre-programmed time constant.

Bit 3 of the Channel Control Word is pre-programmed to select whether timing will automatically initiated, or whether it will be initiated with a triggering edge at the channel's Timer Trigger (CLK/TRG) input. If bit 3 is reset the timer automatically begins operation at the start of the CPU cycle following the I/O Write machine cycle that loads the time constant data word to the channel. If bit 3 is set the timer begins operation on the second succeeding rising edge of the system clock after the Timer Trigger edge following the loading of the time constant data word. If no time constant data word is to follow then the timer begins operation on the second succeeding rising edge of the system clock after the Timer Trigger edge following the control word write cycle. Bit 4 of the Channel Control Word is pre-programmed to select whether the Timer Trigger will be sensitive to a rising or falling edge. Although there is no set-up requirement between the active edge of the Timer Trigger and the next rising edge of the system

clock. If the Timer Trigger edge occurs closer than a specified minimum set-up time to the rising edge of the system clock, the Down Counter will not begin decrementing until the following rising edge of the system clock.

If bit 7 in the Channel Control Word is set, the zero-count condition in the Down Counter, besides causing a pulse at the channel's Time Out pin, will be used to initiate an interrupt request sequence.

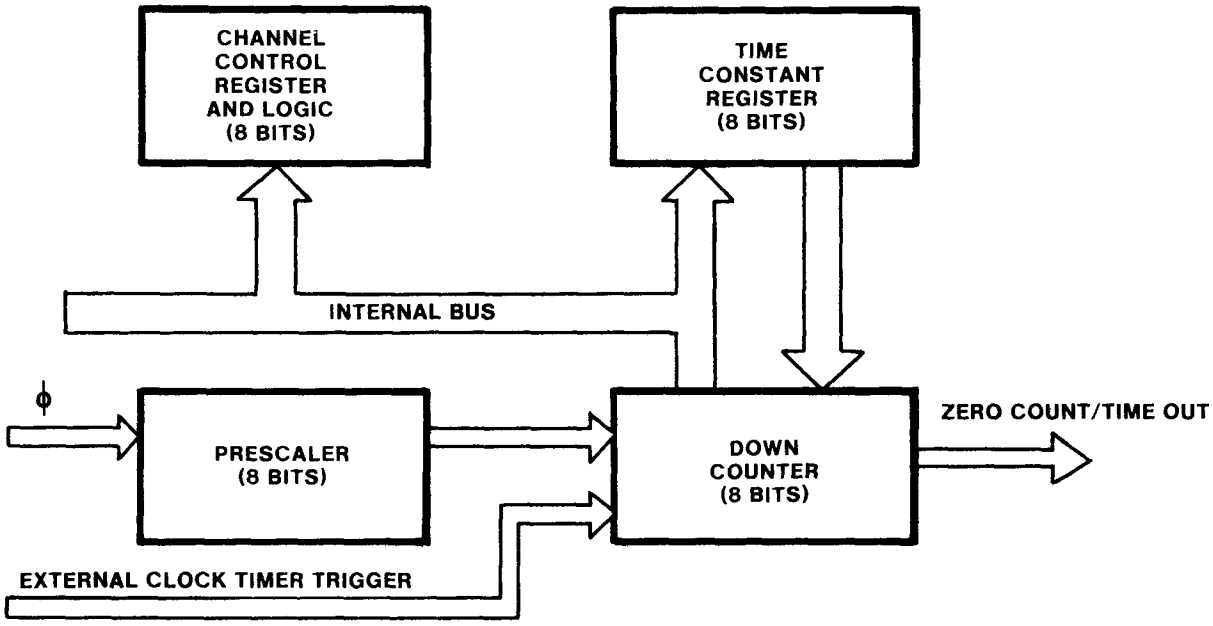


FIGURE E-5 CHANNEL-TIMER MODE

E-5 LOADING CHANNEL CONTROL REGISTER

Before a Z80-CTC channel can begin counting or timing operations, a Channel Control Word and a Time Constant data word must be written to it by the CPU. These words are stored in the Channel Control Register and the Time Constant Register of that channel. In addition, if any of the four channels have been programmed with bit 7 of their Channel Control Words to enable interrupt, an Interrupt Vector must be written to the appropriate register in the CTC. Due to automatic features in the Interrupt Control Logic, one pre-programmed Interrupt Vector suffices for all four channels.

To load a Channel Control Word, the CPU performs a normal I/O Write sequence to the port address corresponding to the desired CTC channel. Two CTC input pins, namely CS0 and CS1, form a 2-bit binary address to select one of four channels within the device. In many system architectures, these two input pins are connected to Address Bus lines A0 and A1, respectively, so that the four channels in a CTC device will occupy contiguous I/O port addresses. A word written to a CTC channel will be interpreted as a Channel Control Word, and loaded into the Channel Control Register, its bit 0 is a logic 1. The other seven bits of this word select operating modes and conditions as indicated in Figure E-6.

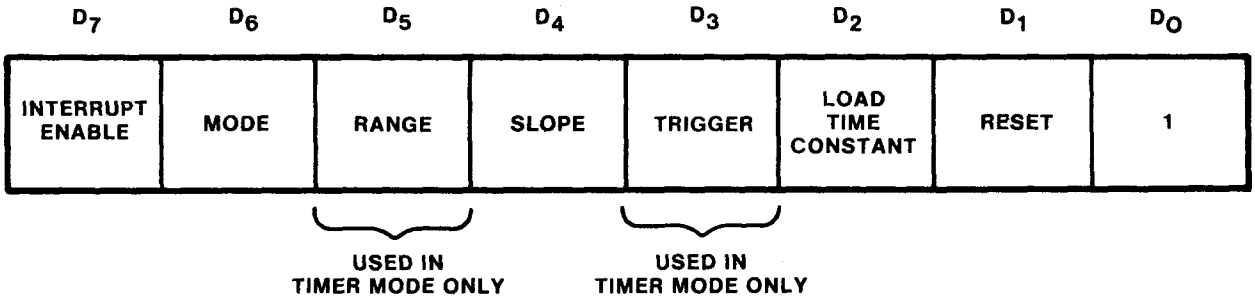


FIGURE E-6 OPERATING MODES AND CONDITIONS

BIT 7=1

The channel is enabled to generate an interrupt request sequence every time the Down Counter reaches a zero-count condition. to set this bit to 1 in any of the four Channel Control Registers necessitates that an Interrupt Vector also be written to the CTC before operation begins. Channel interrupts may be programed in either Counter Mode or Timer Mode. If an updated Channel Control Word is written to a channel already in operation, with bit 7 set, the interrupt enable selection will not be retroactive to a preceding zero-count condition.

BIT 7=0

Channel interrupts disabled.

BIT 6=1

Counter Mode selected. The Down Counter is decremented by each triggering edge of the External Clock (CLK/TRG) input. The Prescaler is not used.

BIT 6=0

Timer Mode selected. The Prescaler is clocked by the System Clock, and the output of the Prescaler in turn clocks the Down Counter. The output of the Down Counter (the channel ZC/TO output) is a uniform pulse train of period given by the product.

$$t_c * P * TC$$

where t_c is the period of System Clock, P is the Prescaler factor of 16 or 256, and TC is the time constant data word.

BIT 5=1

(Defined for Timer Mode only.) Prescaler factor is 256.

BIT 5=0

(Defined for Timer Mode only.) Prescaler factor is 16.

BIT 4=1

TIMER MODE - positive edge trigger starts timer operation.
COUNTER MODE - positve edge decrements the down counter.

BIT 4=0

TIMER MODE - negative edge trigger starts timer operation.
COUNTER MODE - negative edge decrements the down counter.

BIT 3=1

Timer Mode Only - External trigger is valid for starting timer operation after rising edge of T_2 of the machine cycle following the one that loads the time constant. The Prescaler is decremented 2 clock cycles later if the setup time is met, otherwise 3 clock cycles.

BIT 3=0

Timer Mode Only - Timer begins operation on the rising edge of T_2 of the machine cycle followng the one that loads the time constant.

BIT 2=1

The time constant data word for the Time Constant Register will be the next word written to this channel. If an updated Channel Control Word and time constant data word are written to a channel while it is already in operation, the Down Counter will continue decrementing to zero before the new time constant is loaded into it.

BIT 2=0

No time constant data word for the Timer Constant Register should be expected to follow. To program bit 2 to this state implies that this Channel Control Word is intended to update the status of a channel already in operation, since a channel will not operate without a correctly programmed data word in the Time Constant Register, and a set bit 2 in this Channel Control Word provides the only way of writing to the Time Constant Register.

BIT 1=1

Reset channel. Channel stops counting or timing. This is not a stored condition. Upon writing into this bit a reset pulse discontinues current channel operation, however, none of the bits in the channel control register are changed. If both bit 2=1 and bit 1=1 the channel will resume operation upon loading a time constant.

BIT 1=0

Channel continues current operation.

E-6 LOADING TIME CONSTANT REGISTER

A channel may not begin operation in either Timer Mode or Counter Mode unless a time constant data word (See Figure E-7) is written into the Time Constant Register by the CPU. This data word will be expected on the next I/O Write to this channel following the I/O Write of Channel Control Word, provided that bit 2 of the Channel Control Word is set. The time constant data word may be any integer value in the range 1-256. If all eight bits in this word are zero, it is interpreted as 256. If a time constant data word is loaded to a channel already in operation, the Down Counter will continue decrementing to zero before the new time constant is loaded from the Time Constant Register to the Down Counter.

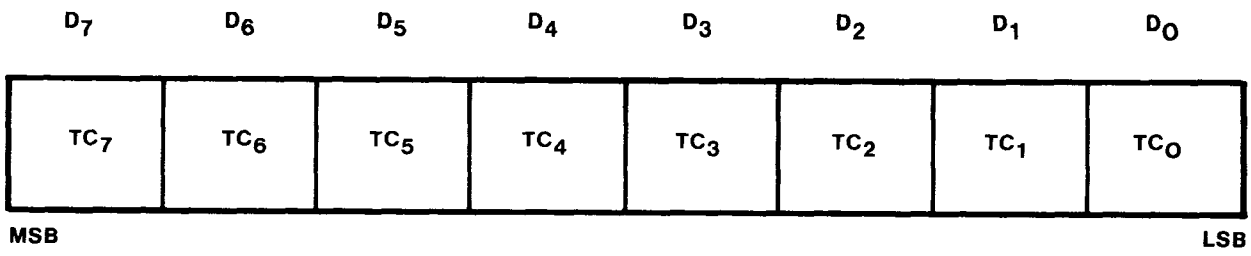


FIGURE E-7 TIME CONSTANT REGISTER

E-7 WRITE CYCLE

Figure E-8 illustrates the timing associated with the CTC Write Cycle. This sequence is applicable to loading either a Channel Control Word, an Interrupt Vector, or a time constant data word.

In the sequence shown, during clock cycle T_1, the Z80-CPU prepares for the Write Cycle with a false (high) signal at CTC input pin RD (Read). Since the CTC has no separate Write signal input, it generates its own internally from the false RD input. Later, during clock cycle T_2, the Z80-CPU initiates the Write Cycle with true (low) signals at a CTC input pins IORQ (I/O Request) and CE (Chip Enable). (Note: M1 must be false to distinguish the cycle from an interrupt acknowledge.) Also at this time a 2-bit binary code appears at CTC inputs CS1 and CS0 (Channel Select 1 and 0), specifying which of the four CTC channels is being written to, and the word being written appears on the Z80 Data Bus. Now everything is ready for the word to be latched into the appropriate CTC internal register in synchronization with the rising edge beginnig clock cycle T_3. No additional wait states are allowed.

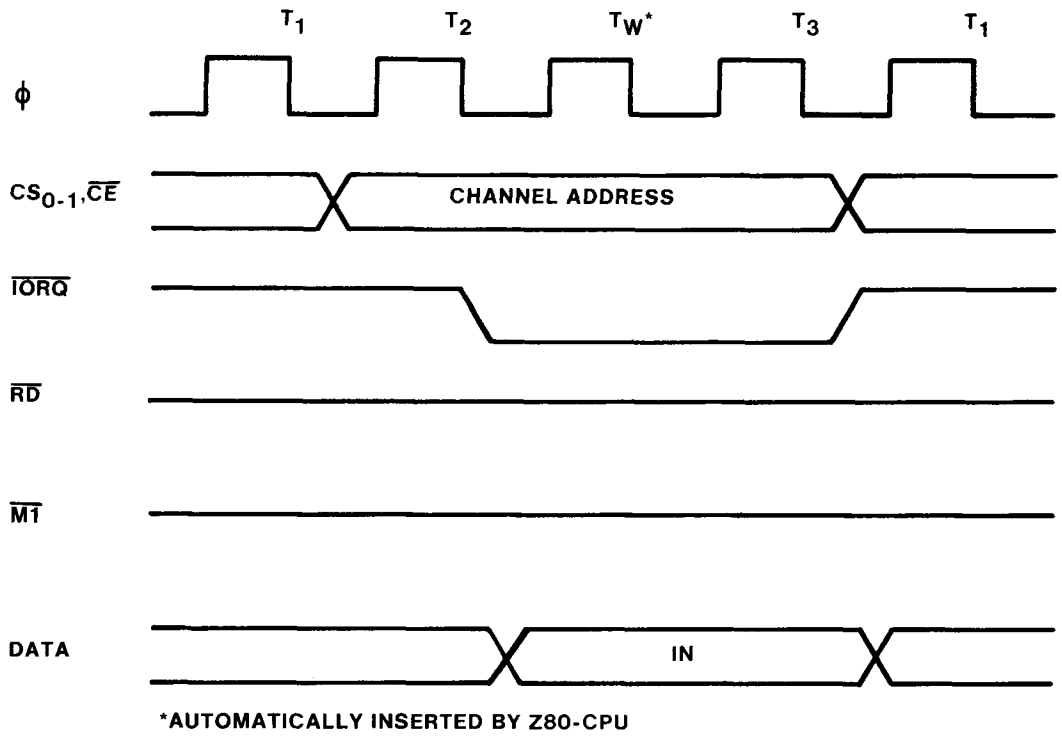


FIGURE E-8 CTC WRITE CYCLE

E-8 READ CYCLE

Figure E-9 illustrates the timing associated with the CTC Read Cycle. This sequence is used any time the CPU reads the current contents of the Down Counter. During clock cycle T_2, the Z80-CPU initiates the Read Cycle with true signals at input pins RD (Read), IORQ (I/O Request), and CE (Chip Enable). Also at this time a 2-bit binary code appears at CTC inputs CS1 and CS0 (Channel Select 1 and 0), specifying which of the four CTC channels is being read from. (Note: M1 must be false to distinguish the cycle from an interrupt acknowledge.) On the rising edge of the cycle T_3 the valid contents of the Down Counter as of the rising edge of cycle T_2 will be available on the Z80 Data Bus. No additional wait states are allowed.

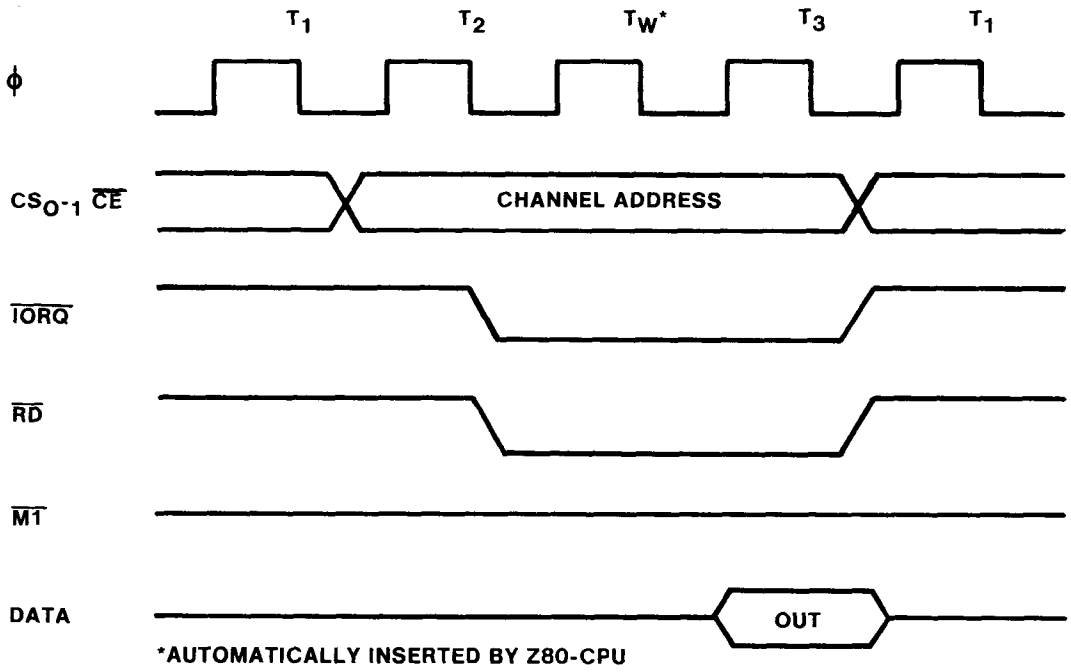


FIGURE E-9 CTC READ CYCLE

E-9 COUNTING AND TIMING

In the Counter Mode, the edge (rising edge is active in this example) from the external hardware connected to pin CLK/TRG decrements the Down Counter in synchronization with the System Clock. This CLK/TRG pulse must have a minimum width and the minimum period must not be less than twice the system clock period. Although there is no set-up time requirement between the active edge of the CLK/TRG and the rising edge of the system clock if the CLK/TRG edge occurs closer than a specified minimum time, the decrement of the Down Counter will be delayed one cycle of the system clock. Immediately after the decrement of the Down Counter, 1 to 0, the ZC/TO output is pulsed true.

E-10 INTERRUPT SERVICING

Each CTC channel may be individually programmed to request an interrupt every time its Down Counter reaches a count of zero. The purpose of a CTC-generated interrupt, as for any other peripheral device, is to force the CPU to execute an interrupt service routine. To utilize this feature the Z80-CPU must be programmed for mode 2 interrupt response. Under the requirements of this mode, when a CTC channel requests an interrupt and is acknowledged, a 16-bit pointer must be formed to obtain a corresponding interrupt service routine starting address from a table in memory. The lower 8 bits of the pointer are provided by the CTC in the form of an Interrupt Vector unique to the particular channel that requests the interrupt.

The CTC's Interrupt Control Logic insures that it acts in accordance with Z80 system interrupt protocol for nested priority interrupt and proper return from interrupt. The priority of any system device is determined by its physical location in a daisy chain configuration. Two signal lines (IEI and IEO) are provided in the CTC and all Z80 peripheral devices to form the system daisy chain. The device closest to the CPU has the highest priority; within the CTC, interrupt priority is predetermined by channel number, with channel 0 having highest priority. According to Z80 system interrupt protocol, low priority devices or channels may not interrupt higher priority devices or channels that have already interrupted and not had their interrupt service routines completed. However, high priority devices or channels may interrupt the servicing of lower priority devices or channels.

In the Timer Mode, a pulse trigger (user-selectable as either active high or active low) at the CLK/TRG pin enables timing function on the second succeeding rising edge of the system clock. As in the Counter Mode, the triggering pulse is detected asynchronously and must have a minimum width. The timing function is initiated in syncroization with the system clock, and a minimum set-up time is required between the active edge of the CLK/TRG and the next rising edge of the system clock. If CLK/TRG edge occurs closer than this, the initiation of the timer function will be delayed one cycle of the system clock.

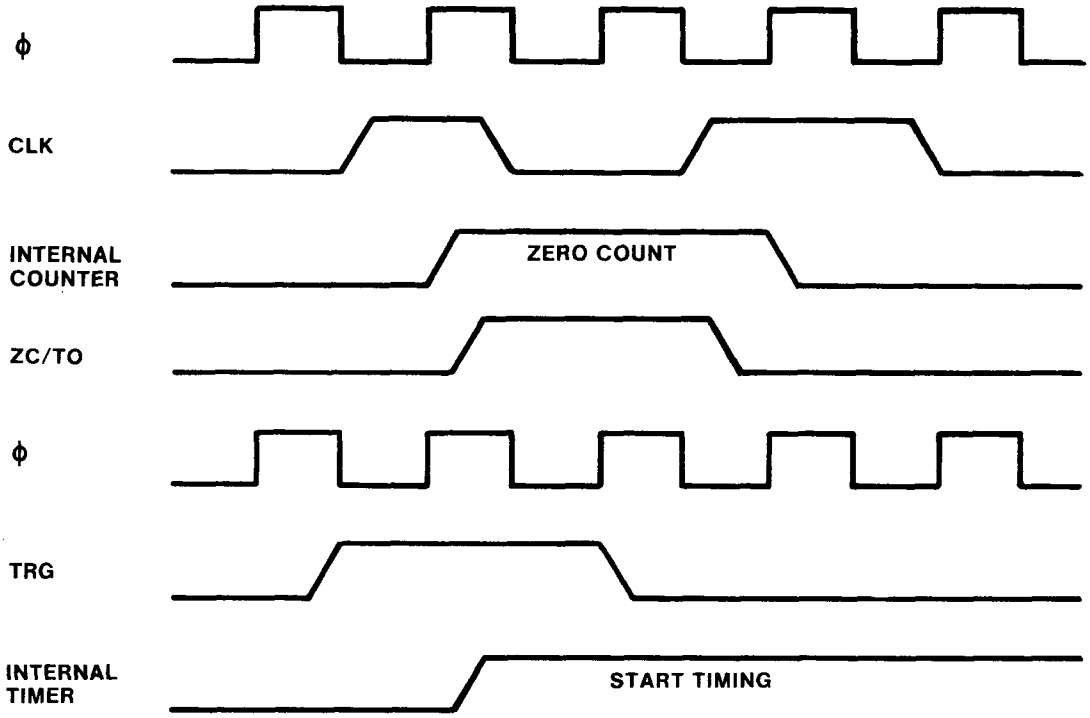
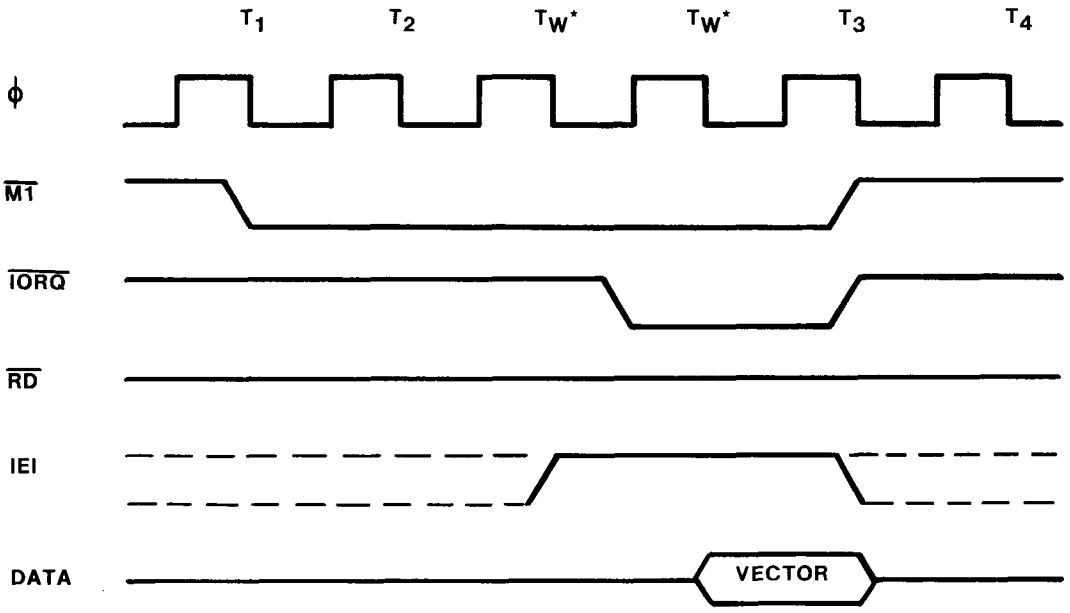


FIGURE E-10 CTC COUNTING AND TIMING

E-11 INTERRUPT ACKNOWLEDGE CYCLE

Figure E-11 illustrates the timing associated with the Interrupt Acknowledge Cycle. Some time after an interrupt is requested by the CTC, the CPU will send out an interrupt acknowledge (M1 and IORQ). To insure that the daisy chain enable lines stabilize, channels are inhibited from changing their interrupt request status when M1 is active. M1 is active about two clock cycles earlier than IORQ, and RD is false to distinguish the cycle from an instruction fetch. During this time the interrupt logic of the CTC will determine the highest priority channel requesting an interrupt. If the CTC Interrupt Enable Input (IEI) is active, then the highest priority interrupting channel within the CTC places its Interrupt Vector onto the Data Bus when IORQ goes active. Two wait states (T_{W*}) are automatically inserted at this time to allow the daisy chain to stabilize. Additional wait states may be added.



*AUTOMATICALLY INSERTED BY Z80-CPU

FIGURE E-11 INTERRUPT ACKNOWLEDGE CYCLE

E-12 RETURN FROM INTERRUPT CYCLE

Figure E-12 illustrates the timing associated with the RETI Instruction. This instruction is used at the end of an interrupt service routine to initialize the daisy chain enable lines for proper control of nested priority interrupt handling. The CTC decodes the two-byte RETI code internally and determines whether it is intended for a channel being serviced.

When several Z80 peripheral chips are in the daisy chain IEI will become active on the chip currently under service when an EDH opcode is decoded. If the following opcode is 4DH, the peripheral being serviced will be re-initialized and its IEO will become active. Additional wait states are allowed.

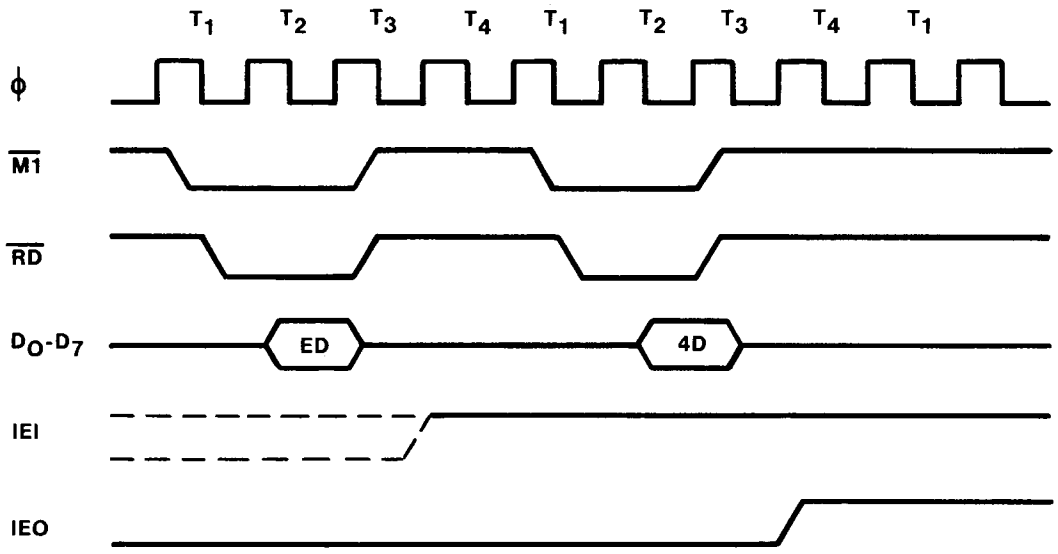


FIGURE E-12 RETURN FROM INTERRUPT CYCLE

APPENDIX F

I/O ADDRESS TABLE

DEVICE	ADDRESS	DATA	DIRECTION
Misc	00	Clicker	0
	01	Beeper	0
	03	Upper Bank Select D7=0=PROM Select =1=CRT Select	0
	05	RAM Bank Select D2 = Page 2 (Optional) D1 = Page 1 D0 = Page 0	0
	06	CTC Reset	0
	07	Device Options Switch	I
	0A	Disk Control 2 Motor On 1 (H) 3 Motor On 0 (H) 4 Terminal Count (H) 5 Reset (H) 6 Door Lock 1 (H) 7 Door Lock 0 (H)	I/O
	0B	Disk Commands, Status, & Data	I/O
	0C	Disk Main Status	I
CTC	20	Printer motor timing	
	21	Printer motor timing	
	22	Real Time Clock	
	23	Printer motor timing	
PIO	30	Keyboard Data - X, Y, & Shift (H)	I
		0 Repeat Key Held Down (H)	I
		1 Keyboard Strobe (H)	0
		6 Disk Data Request (H)	I
		7 Disk Result Interrupt (H)	I
	32	Keyboard Command	
	33	B Command	
VTAC	40	Load Horiz Line Count	0
	41	Load Sync width, delay, interlace	0
	42	Load Scans/data row, char/data row	0
	43	Load Skew bits, data rows/frame	0
	44	Load Scan lines/frame.	0
	45	Load Vertical data start.	0
	46	Load Last displayed data row.	0
	47	Not used	
	48	Read Cursor Row Address.	I
	49	Read Cursor Column Address.	I
	4A	VTAC Reset.	0
	4B	Up Scroll.	0
	4C	Load Cursor Column Address.	0
	4D	Load Cursor Row Address.	0
	4E	Start Timing Chain.	0
	4F	Not used	

DEVICE	ADDRESS		DATA	DIRECTION
Printer				
PIO	50	A Data		I
			0 Right Margin (L)	
			1 Left Margin (L)	
			2 Ribbon Out (L)	
			3 Paper Out (L)	
			4 Cover Open (L)	
			5 Daisy Home (L)	
			6 Ribbon Type (L)	
	51	B Data		I
			0 Select (L)	
			1 Roll Up (L)	
			2 Roll Down (L)	
			3 Line Feed Up (L)	
			4 Line Feed Down (L)	
			5 Paper Load (L)	
			6 Top of Form (L)	
			7 Enable (L)	
	52	A Commands		
	53	B Commands		
	54	Panel LED's		0
			0 Select (H)	
			1 Change Daisy (H)	
			2 Change Ribbon (H)	
			3 Change Paper (H)	
	58	Daisy Motor		0
			0 Phase 1 (H)	
			1 Phase 2 (H)	
			2 Phase 3 (H)	
			3 Phase 4 (H)	
			4 Hold (L)	
	59	Carriage Motor		0
			0 Phase 1 (H)	
			1 Phase 2 (H)	
			2 Phase 3 (H)	
			3 Phase 4 (H)	
			4 Hold (L)	
	5A	Paper Motor		0
			0 Phase 1 (H)	
			1 Phase 2 (H)	
			2 Phase 3 (H)	
			3 Phase 4 (H)	
			4 Hold (L)	
	5B	Ribbon Motor		0
			0 Phase 1 (H)	
			1 Phase 2 (H)	
			2 Phase 3 (H)	
			3 Phase 4 (H)	
			4 Hold (L)	

DEVICE	ADDRESS		DATA	DIRECTION
	5C	Control		0
			0 u Step 1	
			1 u Step 2	
			2 u Step 3	
			3 u Step 4	
			4 Hammer Fire (H)	
			5 Motor Enable (H)	
	5F	Error Display (7 Segment)		0
			0 A (L)	
			1 F (L)	
			2 E (L)	
			3 D (L)	
			4 C (L)	
			5 G (L)	
			6 B (L)	
			7 DP (L)	

Note: Any address not defined is illegal
All bit commands High true are followed by (H).
All bit commands Low true are followed by (H).

APPENDIX G

MEMORY ADDRESS ASSIGNATIONS

The following table and figure provide respectively a listing of the memory locations serving the character rows of the CRT display and a depiction of the address chip layout on the memory PCA.

TABLE G-1

MEMORY ADDRESS TABLE

0000 - 3FFF	16K Program RAM bank 1
4000 - 7FFF	16k Program RAM bank 2
8000 - BFFF	Paged Memory

Pg2	Pg1	Pg0	
0	0	0	16k Program RAM bank 3
0	0	1	16k Program RAM bank 4
0	1	0	16k Program RAM bank 5
0	1	1	16k Program RAM bank 6
1	0	0	16k Program RAM bank 7 (optional)
1	0	1	16k Program RAM bank 8 (optional)
1	1	0	16k Program RAM bank 9 (optional)
1	1	1	16k Program RAM bank 10 (optional)

C000 - FFFF CRT Display Memory

Row	Col	Attribute 1.....80		Data 1.....80	
1		C000	C04F	E000	E04F
2		C100	C14F	E100	E14F
3		C200	C24F	E200	E24F
4		C300	C34F	E300	E34F
5		C400	C44F	E400	E44F
6		C500	C54F	E500	E54F
7		C600	C64F	E600	E64F
8		C700	C74F	E700	E74F
9		C800	C84F	E800	E84F
10		C900	C94F	E900	E94F
11		CA00	CA4F	EA00	EA4F
12		CB00	CB4F	EB00	EB4F
13		CC00	CC4F	EC00	EC4F
14		CD00	CD4F	ED00	ED4F
15		CE00	CE4F	EE00	EE4F
16		CF00	CF4F	EF00	EF4F

TABLE G-1 (continued)

17	D000	D04F	F000	F04F
18	D100	D14F	F100	F14F
19	D200	D24F	F200	F24F
20	D300	D34F	F300	F34F
21	D400	D44F	F400	F44F
22	D500	D54F	F500	F54F
23	D600	D64F	F600	F64F
24	D700	D74F	F700	F74F

Soft Loadable Character Generator (Write Only)

Row	Char 1	Char 128
1	D800	D87F
2	D900	D97F
3	DA00	DA7F
4	DB00	DB7F
5	DC00	DC7F
6	DD00	DD7F
7	DE00	DE7F
8	DF00	DF7F

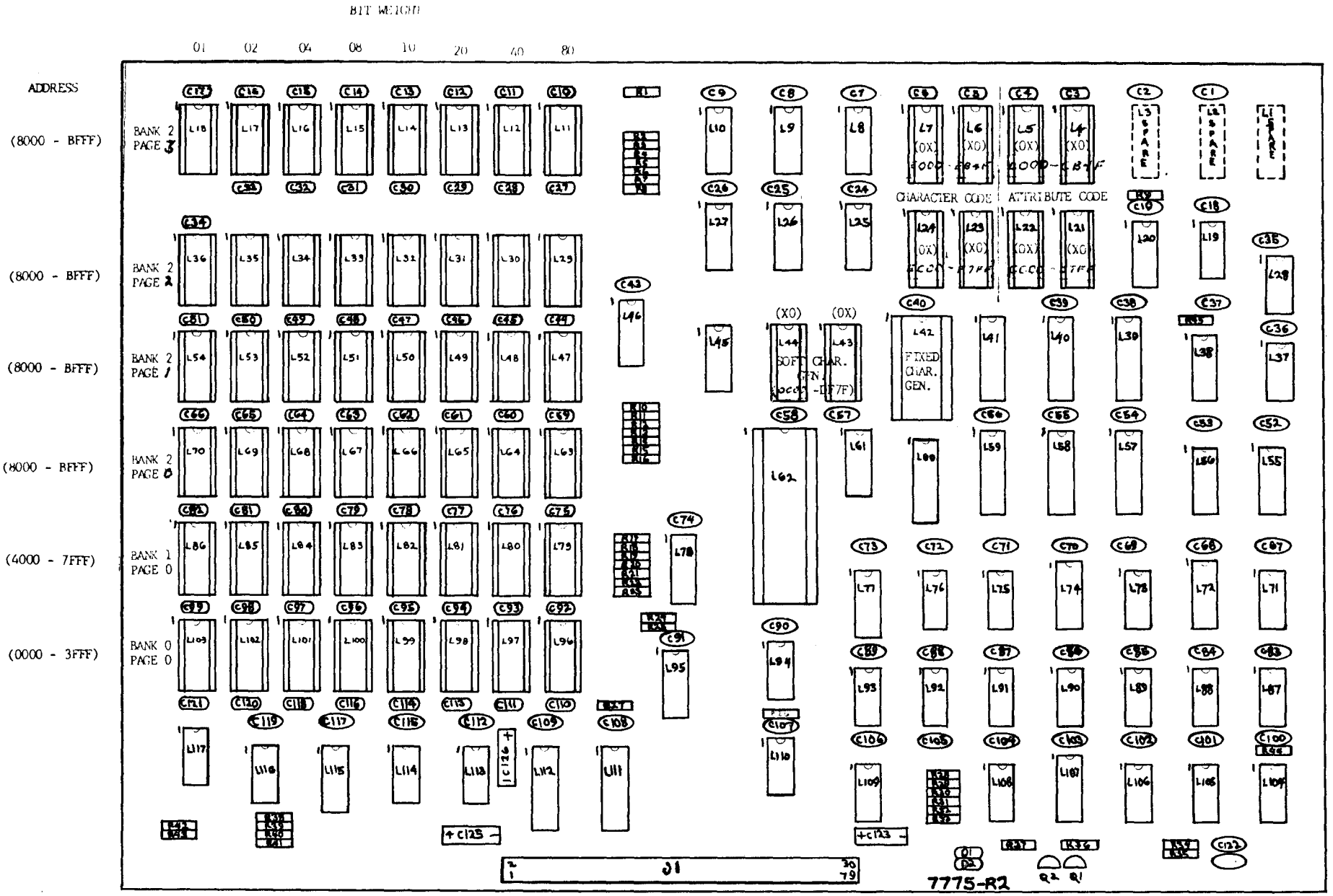


FIGURE G-1 BOARD LOCATION OF MEMORY ADDRESSES

APPENDIX H

SYSTEM DETAILED SPECIFICATION

H-1 CPU SECTION

H-1.1 Z80A CPU

Clock Frequency = 4.0 MHz (T cycle = 250 ns)

H-1.2 Counter Timer Circuit (Z80A - CTC)

Channel 2 is used as a general System Real Time Clock. In the Counter Mode, the channel counts Vertical Sync (each count - 16.7ms) from VTAC in the CRT circuitry. (The VTAC in the CRT circuitry must be initialized before Vertical Sync can be considered accurate.)

Channel 0, 1, & 3 are used in Timer Mode for the timing of the printer stepper motors phase changes. (See Printer Section)

H-1.3 Parallel I/O Controller (Z80A - PIO)

Channel A is used as Keyboard interface and is initialized to the Input mode (See Keyboard Section)

Channel B is used mainly for disk control and is initialized to the Bit control mode with bit assignment as follows:

D0	=	Keyboard Repeat Key Held Down
D1	=	Keyboard Strobe Line
D2-D5	=	Spare
D6	=	Disk Data Request
D7	=	Disk Result Interrupt
		(See Keyboard and Disk Sections)

H-1.4 Interrupts

All interrupts will be in Z80 mode 2 (Vector Interrupt Mode) with priority as follows: (from high to low)

CTC channels 0, 1, 2, 3; System PIO port A, B; Printer PIO port A, B.

H-1.5 Reset

Power On Reset (POR) occurs when power is first turned on and causes the MWPS to initialize to a known state. The program will begin execution at location '0000' and perform hardware forced No-op's until the Bootstrap PROM is accessed at location 'C000' of the Upper Memory Bank. Once the PROM is accessed, the No-op forcing hardware is disabled and normal memory execution can occur.

Condition initialized during POR:

- Upper Memory Bank Points to Bootstrap PROM
- Memory Pages 0, 1, 2 = 0
- CTC is hardware reset
- All printer output control lines = 0
- Floppy Disk Controller and Disk Control Register are reset
- Keyboard Serial Interface Circuitry is reset

Software controlled Floppy Disk Controller reset is done by outputting a '0' to bit 5 of the Disk Control Register at I/O address '0A'.

NOTE: Software must go through the following sequence during initialization to allow the Real Timer Clock to start properly:

1. Initialize VTAC
2. Initialize CTC channel 2
3. Enable CPU interrupts

H-2 MEMORY SECTION

MWPS memory is divided into two sections; the Lower Memory section and the Upper Memory Section.

H-2.1 Lower Memory

The Lower Memory section is the main system memory which consists of 96K bytes with an option of going up to 160K bytes. The additional memory can either be standalone memory or shared by the telecommunication (if any). (See Memory Address Table for detail bank selects)

H-2.2 Upper Memory

The Upper Memory Section is switched between PROM and CRT RAM by bit 7 of output register at '03'. (D7 = 0 PROM, D7 = 1 CRT RAM) Power On Reset sets the pointer to PROM.

The CRT RAM is further divided into 3 sections:

1. Character Control Section (2K bytes)
2. Attribute Control Section (2K bytes)
3. Soft Character Generator (1K bytes)

(See Memory Address Table for detail decoding)
(See Display Section for using CRT RAM memories)

H-3 DISPLAY SECTION

This section controls the presentation of video data stored in CRT RAM, to the CRT monitor. The CRT RAM is divided into 2K bytes of Character Control, 2K bytes of Attribute Control and 1K bytes of Soft Character Generator.

H-3.1 Character Control

The Character Control byte has the following bit assignments:

MSB	D7	D6	D5	D4	D3	D2	D1	D0	LSB

D7 = Soft Character/Standard Character SEt
D6-D0 = Character Code

Standard Character Set -- With D7 = 0, the character code that follows is used to decode the 128 characters from the standard character set.

Soft Character Set -- With D7 = 1, the character code that follows is used to decode the 128 characters from the soft character set which is software loadable and is used for special characters and/or Character Set Graphics.

H-3.2 Attribute Control

The Attribute Control byte has the following bit assignment:

D7 = Underscore - underlines character on scan line 10.
D6-D4 = Box Graphics - draw horizontal and vertical line segments.
D3,D2 = Display Control - control intensity and reverse video.
D1,D0 = Superscript and Subscript Control - moves matrix up or down.

H-4 VIDEO TIMER AND CONTROLLER

The heart of the CRT Control circuitry is the CRT Video Timer and Controller (VTAC) Integrated Circuit. The VTAC contains the major portion of the logic required to generate the timing signals necessary to present video data on the CRT monitor.

The VTAC must be initialized after power on by software. The following output commands must be executed to initialized the VTAC:

I/O ADDRESS	OUTPUT DATA (HEX)	FUNCTION
'40'	'63'	Horizontal Character Count (=100)
'41'	'26'	Mode (non interlaced) Horizontal Sync Width (=4) Horizontal Sync Delay (=6)
'42'	'55'	Scans/Data Row (=11) Character/Data Row (=80)
'43'	'D7' ('D8')	Skew bits (=2) Data Rows/Frame (-24)*
'44'	'17'	Scans/Frame (=290)
'45'	'14'	Vertical Data Start (=20)
'46'	'17' ('18)	Last Displayed Data Row (=24)*

The VTAC provides the following commands:

Output Address	Function
4A	Blank the Screen (Reset)
4B	UnScroll
4E	Unblank the Screen (Start Timing Chain)

The Vertical Scrolling without the need to shift the entire RAM is provided by the 'Up Scroll' and 'Last Displayed Data Row' commands. Upward Scrolling is accomplished by issuing an 'Up Scroll' command (OUT '4B') or by loading the incremented Last Displayed Data Row Count (OUT '46'), then the data of the last displayed data row is changed.

When downward scrolling, the decremented Last Displayed Data Row Count is loaded and the previous last displayed data row is then changed. The data row count must be modulo 24 when using this Scrolling method. Because of this, the horizontal line graphics in the 25th row cannot be used.

Cursor is generated through the VTAC. The location of the cursor can be read and written by the following I/O commands:

I/O Address	Function
48	Read Cursor Row Address
49	Read Cursor Column Address
4C	Load Cursor Column Address
4D	Load Cursor Row Address

-- Cursor appears on scan lines 9 and 10 with high intensity and blink rate of 1.8 Hz (75/25 duty cycle).

NOTES: All the parameters can be changed at any time during operation.

* When the box grahics feature is to be used the output data in parenthesis is used.

--- To insure proper initialization of the registers, the following sequence should be employed.

I/O Address	Commands
4E	Start Timing Chain
4A	Reset
40	Load Register 0
:	:
46	Load Register 6
4E	Start Timing Chain

H-5 PRINTER SECTION

The printer consists of four motors -- paper motor, carriage motor, ribbon motor and daisy motor. Each stepper motor is controlled by 4 phase signals and hold line. CTC channels 0, 1, and 3 are used in the timer mode for timing the stepper motor phase changes.

Four Write-Only Register are used for the four motors. Their Output addresses are:

I/O Address	Function
58	Daisy Motor Control
59	Carriage Motor Control
5A	Paper Motor Control
5B	Ribbon Motor Control

Each register has bit assignments as follows:

Data Bits	Function
D0	Phase 1
D1	Phase 2
D2	Phase 3
D3	Phase 4
D4	Hold

Register '5C' controls micro-stepping, hammer fire and motor enable, with bit assignments as follows:

Data Bits	Function
D0	Phase 1
D1	Phase 2
D2	Phase 3
D3	Phase 4
D4	Hammer Fire
D5	Motor Enable

When first power up all phases will be held low, all motors stay in a hold mode, and hammer stays inactive. Power of the motors is disabled by the Motor Enable bit.

There are 6 switches on the switch panel -- Select, Roll up, Roll Down, Line Feed Up, Line Feed Down and Top of Form. All of these signals are fed into Printer PIO port B. Other switching signals include -- Ribbon Type, Paper Load and Cover Open.

There are 5 sensors -- Right Margin, Left Margin, Ribbon Out, Paper Out and Daisy Home. These sensing signals are input to CPU through Printer PIO port A.

Port assignment of Printer PIO is shown as follows:

PORT	DATA BIT	INPUT SIGNALS
A	D0	Right Margin
	D1	Left Margin
	D2	Ribbon Out
	D3	Paper Out
	D4	Cover Open
	D5	Daisy Home
	D6	Ribbon Type
B	D0	Select
	D1	Roll Up
	D2	Roll Down
	D3	Line Feed Up
	D4	Line Feed Down
	D5	Paper Load
	D6	Top of Form
	D7	Enable

Four LED's are placed on the switch panel to indicate necessary changes need. The Output register is at '54' with bit assignment as follows:

DATA BIT	INPUT SIGNALS
D0	Select
D1	Change Daisy
D2	Change Ribbon
D3	Change Paper

An Error Display is placed at the back of the unit. The Output register used to control this 7-segment display is at output address '5F'. The seven segments and the left decimal point are controlled by each bit in that register. The bit assignment is shown as follows:

DATA BIT	SEGMENT NAME
D0	A
D1	F
D2	E
D3	D
D4	C
D5	G
D6	B
D7	DP

There is a character print counter. It is activated by doing an OUT command to port '5E'.g.

H-6 DISK SECTION

The MWPS can support up to 2 double-sided, double-density Mini-Floppy Disks. These drives will be controlled by NEC 765 Floppy Disk Controller (FDC).

H-6.1 Mini Floppy Drive Characteristics

Rotational Speed	300 RPM
Rotational Period	200 ms
Average Access Time	463 ms
Average Latency	100 ms
Disk Transfer Rate	250k bits/sec
Access Time Track to Track	25 ms
Head Settling Time	10 ms
Disk Motor Start Time	1 sec
Tracks	35
Sectors/Track	16
Bytes/Sector	256
Bit Cell Time	4 us
Byte Rate	32 us
Time/Sector (MFM Recording Method)	11.9 ms (8.19 ms for data (3.17 ms for gap)

H-6.2 Mini Floppy Disk Controller

The Floppy Disk Controller (FDC) is a programmable device, which is used to interface the CPU to the mini-floppy disk drives.

The Floppy Disk Controller is capable of accepting 15 different commands:

1. Specify	6. Read Data	11. Format a Track
2. Sense Drive Status	7. Read Deleted Data	12. Read ID
3. Recalibrate	8. Write Data	13. Scan Equal
4. Sense Interrupt Status	9. Write Deleted Data	14. Scan High/Equal
5. Seek	10. Read A Track	15. Scan Low/Equal

Each command requires multiple 8-bit bytes to specify the operations. The command words are sent to FDC by OUT 'OC' instructions. To terminate the commands completely, the processor must read the Status Register by IN 'OC' instructions.

The Main Status Register can be accessed anytime by IN 'OB' for handshaking with the processor.

Format -- The recording method used is MFM recording
-- Soft Sectored Format is fixed by FDC
-- Each track has a Track Address Field after the index pulse. This field contains the Index Address Mark, which the FDC uses to determine the track number.

-- Each of the 16 sectors has an ID field and a Data field. The ID field contains the cylinder no., side no., sector no., and the sector size. This ID field is supplied by the processor during disk formatting, and allows the disk to be formatted with non-sequential sector numbers.

-- The Data Field has 256 bytes of data and a 2 byte CRC code.

Data Transfer

-- Read Data -- uPD 765 generates DRQ's when each byte of data is available. DRQ comes in through System PIO port B bit 6. The CPU must read the FDC and write the byte it received to memory with an INI 'OC'. The time between bytes is limited to 26 us. The CPU must terminate the FDC operation by setting the FDC Terminal Count at bit 4 of register 'OA'.

-- Write Data -- The CPU must read a byte from memory and write it to the FDC with an OUTI 'OC'. A Terminal Count is also necessary to stop the operation.

-- The FDC will generate an interrupt through bit 7 of System PIO port B. Bit 7 must be masked, during PIO initialization, to generate an interrupt upon going high. This interrupt informs the CPU that FDC has completed the Execution phase. The interrupt is cleared when the first byte of data is read during the following Result Phase.

H-6.3 Disk Control Register

An 8-bit output control register with I/O address 'OA' has the following bit assignments:

D7	=	DL0	(Door Lock 0)
D6	=	DL1	(Door Lock 1)
D5	=	Reset Disk	(FDC Reset)
D4	=	Disk TC	(Terminal Count)
D3	=	MON0	(Motor On 0)
D2	=	MON1	(Motor On 1)
D1,D0	=	Spare	

Note that the contents of this register can be read back by an IN 'OA' instruction.

H-6.4 Keyboard Section

The keycode is input through the System PIO port A which should be set up in the Input mode (mode 1). The bit assignment of port A is as follows:

Data Bit	Input
A7	Shift
A6	K6
A5	K5
A4	K4
A3	K3
A2	K2
A1	K1
A0	K0

Whenever a key is struck on the keyboard, the PIO would give out an interrupt. Keycode should be read in the interrupt routine to reset the Ready line of port A. This is done by executing the IN'30' instruction.

For proper initialization of the PIO, two precautions must be taken:

-- Must disable the system interrupt before initialization
-- Must do a dummy read after initialization to set the Ready Line

Every key on the keyboard is a repeat key. The repeat line comes in through Bit 0 of the System PIO port B. This Repeat Key Held Down signal will remain high as long as a key is held down.

The keyboard also provides a N key Rollover capability. That is to say when a key is struck while other keys are being held down, the keyboard will be able to output the latest keycode that comes in.

The keyboard also contains a clicker which will sound whenever an OUT '00' is executed. This command will be issued by the software whenever a keystroke is accepted. A beeper will sound whenever an OUT '01' is executed.

APPENDIX J

FLOPPY-DISK AND DISK-DRIVE SPECIFICATION

PARAMETER	CHARACTERISTICS
Media	ANSI standard 5 1/4-inch diskette
Number of Tracks	40/51 70/52
Track Density	48 TPI
Start/Stop Time	0.5 sec
Rotational Speed	300 rpm $\pm$ 1 1/2%
Average Latency	100 msec
Head Loading time	35 msec
Access time	5 msec, track-to-track
Head settling time	15 msec
Access time	15 msec
Head Life	20,000 hours
Media Life	3×10^6 passes on single track
Recording method	FM, MFM, M^2FM
Recording Density (FM)	2810/5620 bpi
Flux density	5620 fci max.
Data-transfer rate	125K/250K bits/sec.
Power-up Delay	0.5 sec
Height	3.25 inches (8.255 cm)
Width	5.75 inches (14.605 cm)
Length	7.5 inches (19.05 cm)
Weight	3.0 pounds (1.36 kg)
Power	+12 VDC $\pm$ 5% 0.8A (1.5A surge)
	+5 VDC $\pm$ 5% 0.4A
Typical Power Dissipation	12W Operating
	6W Standby
Operating Temperature	$40^\circ F$ to $115^\circ F$ ($4.4^\circ C$ to $46.1^\circ C$)
Storage Temperature	$-40^\circ F$ to $160^\circ F$ ($-40^\circ C$ to $70^\circ C$)
Operating Humidity	20% to 80% (noncondensing)
Storage Humidity	5% to 95% (noncondensing)
Operating altitude	-500 ft to 10,000 ft (-152.4m to 3,048m)
Storage altitude	-1000 ft to 50,000 ft (-304.8m to 15,240m)
Vibration and Shock (Operating)	6 to 600 Hz, 0.5g

APPENDIX K

DEPOT-LEVEL CHECKS AND ADJUSTMENTS

The following checks and adjustments are to be performed at depot-level only.

K-1 PRINT WHEEL HOME POSITION ADJUSTMENT

This adjustment to be performed if the home character position is off by one or less.

1. Rotate front plate:

   a) De-select printer.
   b) Put carriage assembly in service position.
   c) Remove print wheel.
   d) Loosen the screws on the front of the motor (see Figure 5-10, Chapter 5).
   e) Rotate front plate to adjust and then tighten screws.

NOTE

Turn clockwise if lower case o was to the left of home position and vice versa.

   f) Put print wheel on.
   g) Put print head in operating position.

CAUTION

Never leave carriage in service position when selecting printer.

h) Select printer.

i) Observe home position alignment.

NOTE

Re-adjust, if necessary, to get alignment at home position.

2. Perform Final Adjustment

a) Turn power OFF.

b) Loosen screws on the rear of motor.

c) Put carriage in normal print position to square off print wheel motor assembly.

d) Tighten screws on the rear of motor.

K-2 PRINT SOLENOID ARM AND LAMINATION ADJUSTMENT

1. To adjust the print solenoid arm with respect to the face of the lamanation loosen the coil assembly mounting screws (see Figure 5-11, Chapter 5).

2. Push print solenoid arm forward (toward platen) as far as possible and hold.

3. Move the coil assembly until its laminations are touching and parallel with the print solenoid arm surface.

4. Tighten mounting screws while holding coil in place.

K-3 PRINT SOLENOID ARM AND HAMMER CHECK

Check the print solenoid arm and hammer alignment to ensure that the arm crosses the hammer as shown in Figure K-1.

K-4 PRINT SOLENOID ARM AND HAMMER ALIGNMENT

1. To adjust, loosen the two screws on print yoke mounting bracket (see Figure K-2) and rotate print-yoke assembly about daisy motor until the print solenoid arm is in the position shown in Figure K-1.

2. Recheck hammer-to-platen adjustment.

K-5 RIBBON PLATFORM CHECK

Check that 0.0937 to 0.125 inch (0.238 to 0.317 cm) exist between ribbon cartridge and damper-bracket ears.

NOTE

The same gap must exist on both sides.

K-6 RIBBON PLATFORM ADJUSTMENT

1. Loosen the two screws under the platform (see Figure K-3).

2. Move the platform so that 0.0937 to 0.125 inch (0.238 to 0.317 cm) exist between ribbon cartridge and damper-bracket ears.

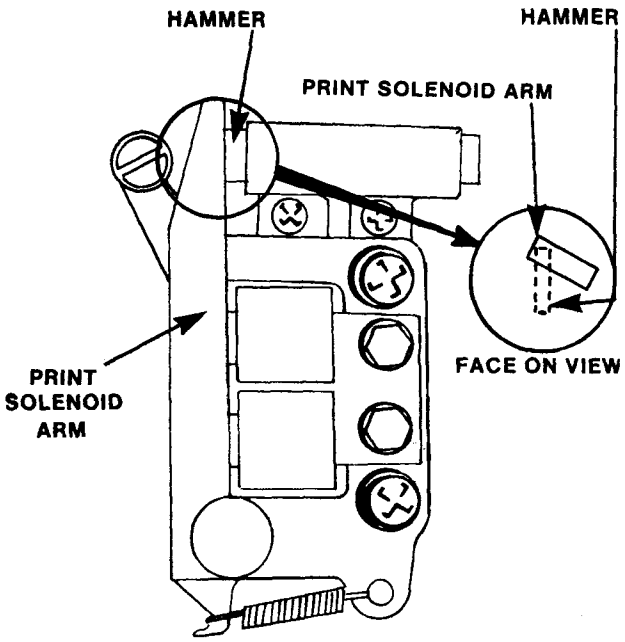


FIGURE K-1 PRINT SOLENOID ARM AND HAMMER CHECK

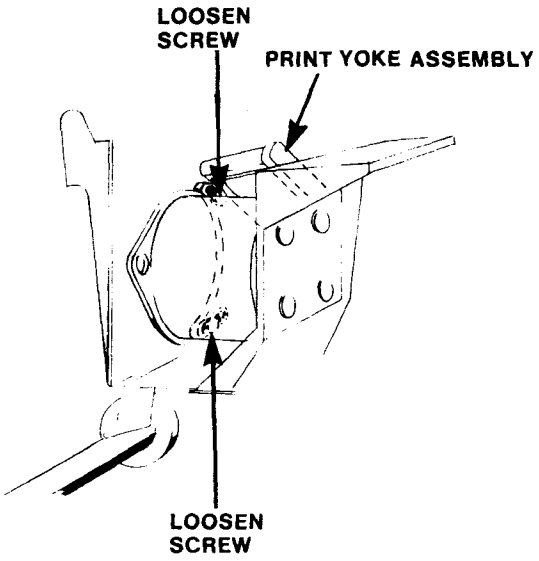


FIGURE K-2 PRINT SOLENOID ARM AND HAMMER ADJUSTMENT

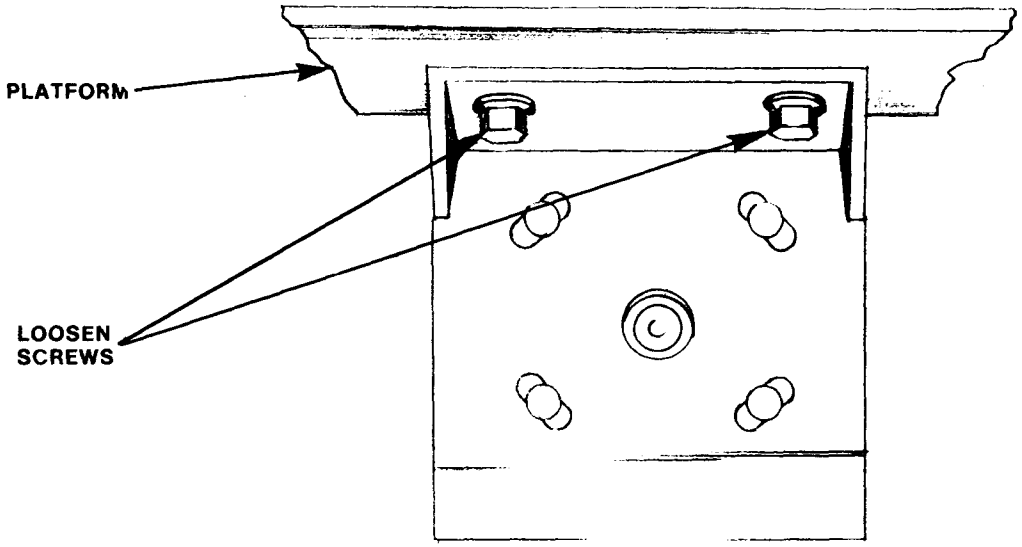


FIGURE K-3 RIBBON PLATFORM ADJUSTMENT

NOTE

The same gap must exist on both sides.

K-7 RIBBON DRIVE CHECK

1. Remove ribbon cartridge.

2. Check that the ribbon drive has 8-to-12 ounces (224-to-336 grams) of spring tension (measure with gram gauge WL #726-4417 at the base of spike driver). See Figure K-4. Push at base of spike driver as shown in Figure K-4.

NOTE

Take reading when spike driver begins to move from the pressure applied by the gram meter.

K-8 RIBBON DRIVE ADJUSTMENT

1. Open grip ring and rotate it around motor (see Figure K-5).

NOTE

From a top view rotate grip ring clockwise to increase tension and counter-clockwise to decrease tension.

2. Adjust for 8-to-12 ounces (224-to-336 grams).

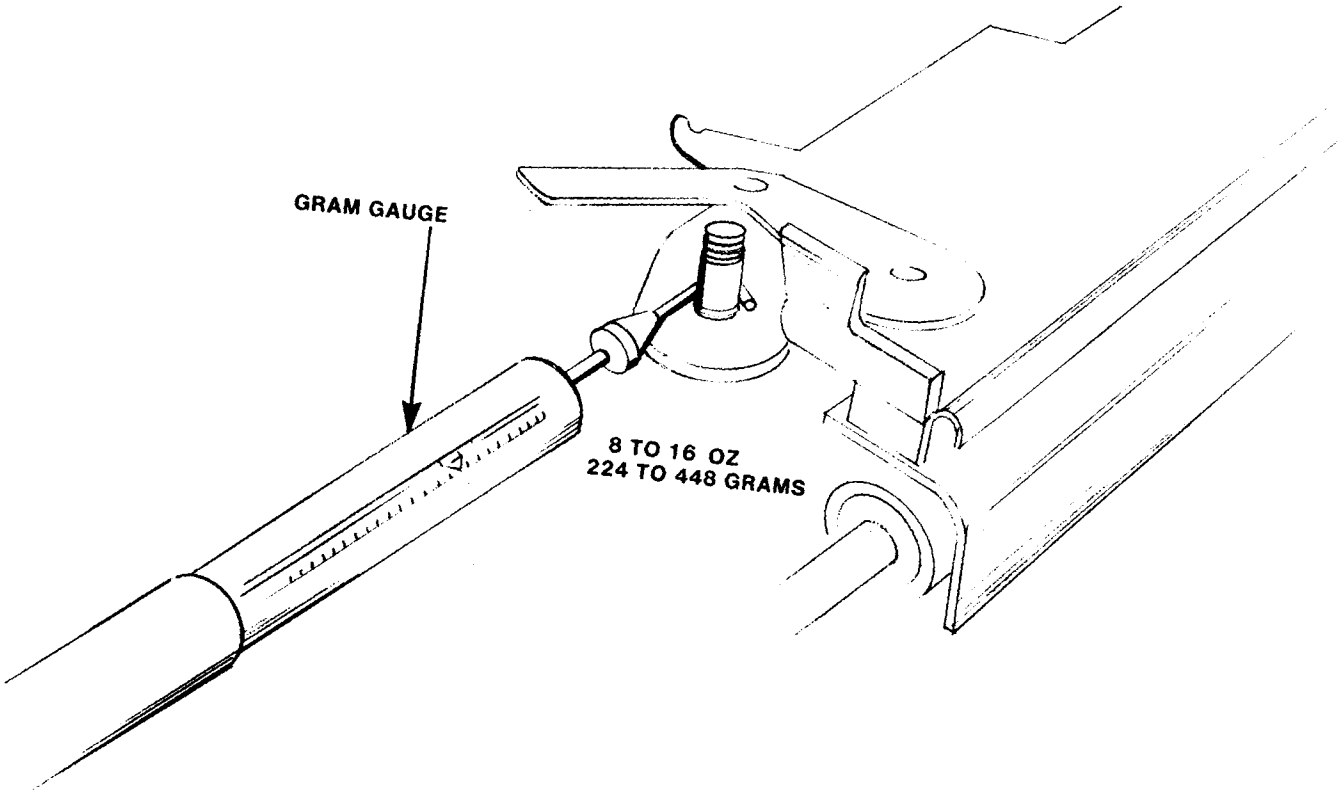


FIGURE K-4 RIBBON DRIVE SPRING TENSION CHECK

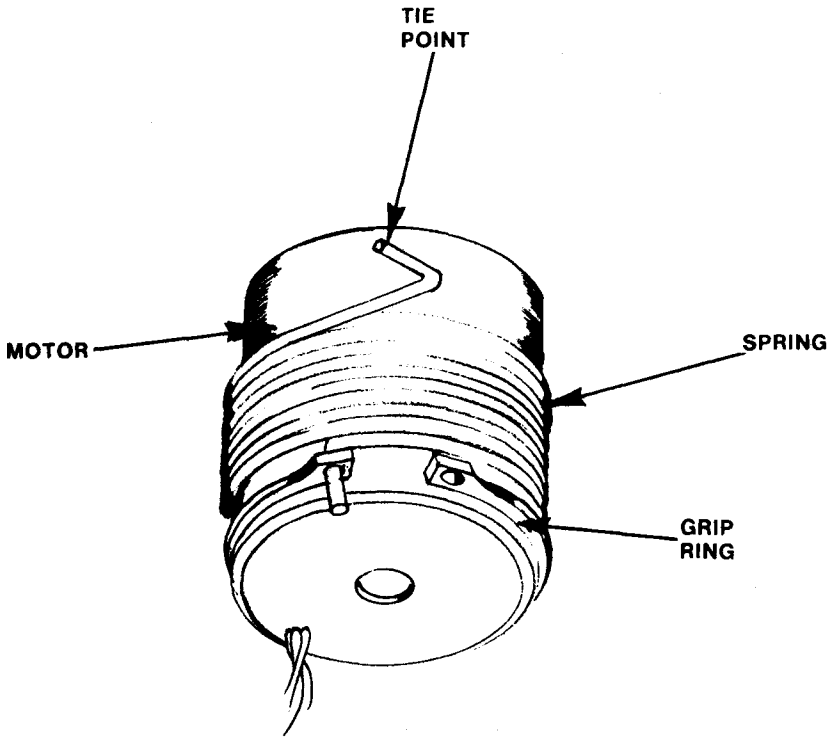


FIGURE K-5

APPENDIX L

RECOMMENDED SPARES LIST

The following comprises lists of system components recommended for availability at the maintenance levels of branch, area, and depot.

BRANCH

WANG PART NO.	DESCRIPTION
210-7456	CRT electronics PCA, 12" Mon.
210-7775-A	CRT/Memory PCA
210-7776-A	PRN PCA
210-7777-A	CPU (Disk, Prn) PCA
278-4022	Disk Drive, 5 1/4 inch Mini-Floppy w/door lock
279-9000-22	Printer Head Assy./with carriage
279-9000-26	Carriage Motor Assy.
279-9000-27	Paper Drive Motor Assy.
279-9000-34	P.S. Reg. Bd. & Heat Sink
360-1016-SB	Fuse, Picofuse, 1A 125V (P.S.-18V)
360-1031-SB	Fuse, Picofuse, 3A, SB, (AC input 115V)
360-1154	Fuse, Picofuse, 1A 125V (P.S. - 18V)
360-1155	Fuse, Picofuse, 2A 125V (PRT PCB-36V)
360-1156	Fuse, Picofuse, 4A 125V (PRT PCB-36V)
360-0026	MPI-1-35026-001 LED, red, Disk (TIL 220)
375-2110-4	Sensor, Home/Ribbon
375-2120	Sensor, R & L carriage and Paper out
377-0341	2114 RAM, 1024 x 4 bit Static RAM
377-0345	4116 RAM, 16K x 1 bit Dynamic RAM
725-2635	Keyboar Assy., Keytronic
726-8069	MPI-1-50500-001 Belt, Disk Drive

AREA

WANG PART NO.	DESCRIPTION
220-1505	Keyboard Cable Assy.
270-0689	12" Monitor and Frame Assy., Tilting
271-1222	Kybd & Brkt Plate Assy., Wang
279-0441	Sw. Assy, Kbd, Wang, Strt.
279-0442	Sw. Assy, Kbd, Wang, Angl.
279-9000-17	Spike Driver Assy.
279-9000-20	Platen Assy.
279-9000-32	P.S. Assy.
360-1016-33	Switch Panel Assy.
360-1031-35	Sw. Assy., Cover Open
420-1033	Cable, Carriage Drive
465-1236	Guide, Paper
220-3139	Printer Head Flex Cable Assy.
400-1012	Fan, Muffin, 50 CFM
726-8070	MPI-3-29003-XXX PCB Assy.

DEPOT

WANG PART NO.	OEM NO	DESCRIPTION
210-7778		P.S. Regulator PCA
210-7779-A		Keyboard PCA, Wang
210-7782		Sw. Panel PCA (Printer)
220-1472		Floppy Power Cable Assy.
220-3131		Floppy Logic Cable Assy.
220-0262		CRT Cable Assy
270-0689		12" Monitor & Frame Assy., Tilting
270-3182		CPU/Printer Driver Pwr. Cable Assy.
279-0441		Sw. Assy, Kbd, Wang, Straight
279-0442		Sw. Assy, Kbd, Wang, Angled
279-9000-20		Platen Assy.
279-9000-21		Paper Guide Assy.
279-9000-70		CRT Assy.
279-9000-91		Speaker Assy.
320-0055		Coil, Print Solenoid
323-0010		Counter, Printer Char., 6 Dig., 12V
325-0059		Switch, DPST, Rocker
325-2118		Switch, Slide, DPDT, 115/230v
325-2303		Micro SW w/activator, cover, 311SM5-T
325-2305		Micro SW, SW Panel, 11SM1
325-2313		Switch Submin, light force, 10 Amp
340-0017	DL707	7-Segment Display
340-0108		Tube, CRt, 12"
360-0016		Fuse holder, Shock Safe, 3AG
360-1154		Fuse, Picofuse, Littlefuse, 1A 125V
360-1155		Fuse, Picofuse, 2A, 125V
360-1156		Fuse, Picofuse, 4A, 125V
370-0026		Lamp, Red, LED
375-1000		Transistor, MPS 6516, Sil.
375-1004		Transistor, 2N3646, NPN
375-1050		Transistor, SPS6551
375-1052		Transistor, 2N 6386
375-1053		Transistor, RCA8203A
375-1062		Transistor, MPS6514
375-1068		Transistor, 2N3903
375-1069		Transistor, 2N3905
375-2110-4		Sensor, Daisy Home/Ribbon
375-2120		Sensor, R & L carriage/paper out
376-0482	MC 10125	ECL to TTL translator
376-0483	MC 1658	Voltage Cont. Multivibrator
370-0026	MPI-1-35026-001	LED, Red, Disk, (TIL 220)
377-0314	CD 4050	Hex Buffer, non-inv., CMOS
377-0341-L	2114	1024 x 4 bit static RAM
377-0345-T	4116	16K x 1 bit dynamic RAM
377-0368	Z80Z CPU	CPU, LSI
377-0371	Z80A CTC	Counter/Timer Control, LSI
377-0372	CRT 5027	VTAC (Video Timer Controller)
377-0373	Z80 PIO	PIO, LSI
377-0381	uPD 765	NEC Floppy Disk Controller

EPROM (continued)

377-0391	AY-3-4592	Keyboard Encoder
377-0395	IM 6402	UART, CMOS low pwr., 1 MHZ
377-0398	2716 *	16K x 1 bit (2k x 8) EPROM, 5V type
378-3035	2708	EPROM, CRT character generator
378-4225		EPROM, Pwr up/IPL (5110)
400-0037		Motor, Paper feed, stepping
400-0038		Motor, Ribbon, stepping
400-0056		Motor, Daisy, stepping, 8VDC/2A
400-0057-UM		Motor, Carriage, stepping, 1.4V/3.8A
420-1033		Cable, Carriage drive
449-0425		Platen gear, 32P/54T
451-2314		Cover, Printer
458-0374		Spike, Ribbon drive
458-0398		Hammer, Printer
458-0927		Shim, Carriage brkt., .005 thick
458-0928		Shim, Carriage brkt., .010 thick
654-3006		Housing, 40-40 ZIF, side lever
654-3007-R		Contact pin, ZIF conn.
725-2635		Keyboard, Keytronic
726-8069	MPI-2-27004-001	Belt, Disk Drive, Black neoprene
726-8070	MPI-3-29003-XXX	PCB Assy., Disk

MPI mini-disk drive-

MPI-2-35000-001	Track Zero Assembly
MPI-2-35001-002	Index sensor Assy.
MPI-3-35006-001	Rt hand guide/Write Protect
MPI-60000-016	Connector (1/2 of J4)
	Pin, Connector, J4

*Texas Instrument equivalent for 16K, 5-volt type EPROM is TMS 2516

APPENDIX M

SYSTEM SCHEMATICS

The engineering drawings contained in this appendix are the schematics for the principal electronic assemblies serving the Wangwriter Model 5503 system. Drawing numbers, and nomenclature, are as follows:

7456	Electronics for 9" and 12" Monitor
7775	CRT/Memory Board
7776	Printer Driver Board
7777	CPU/Disk/Keyboard
7778	Regulator